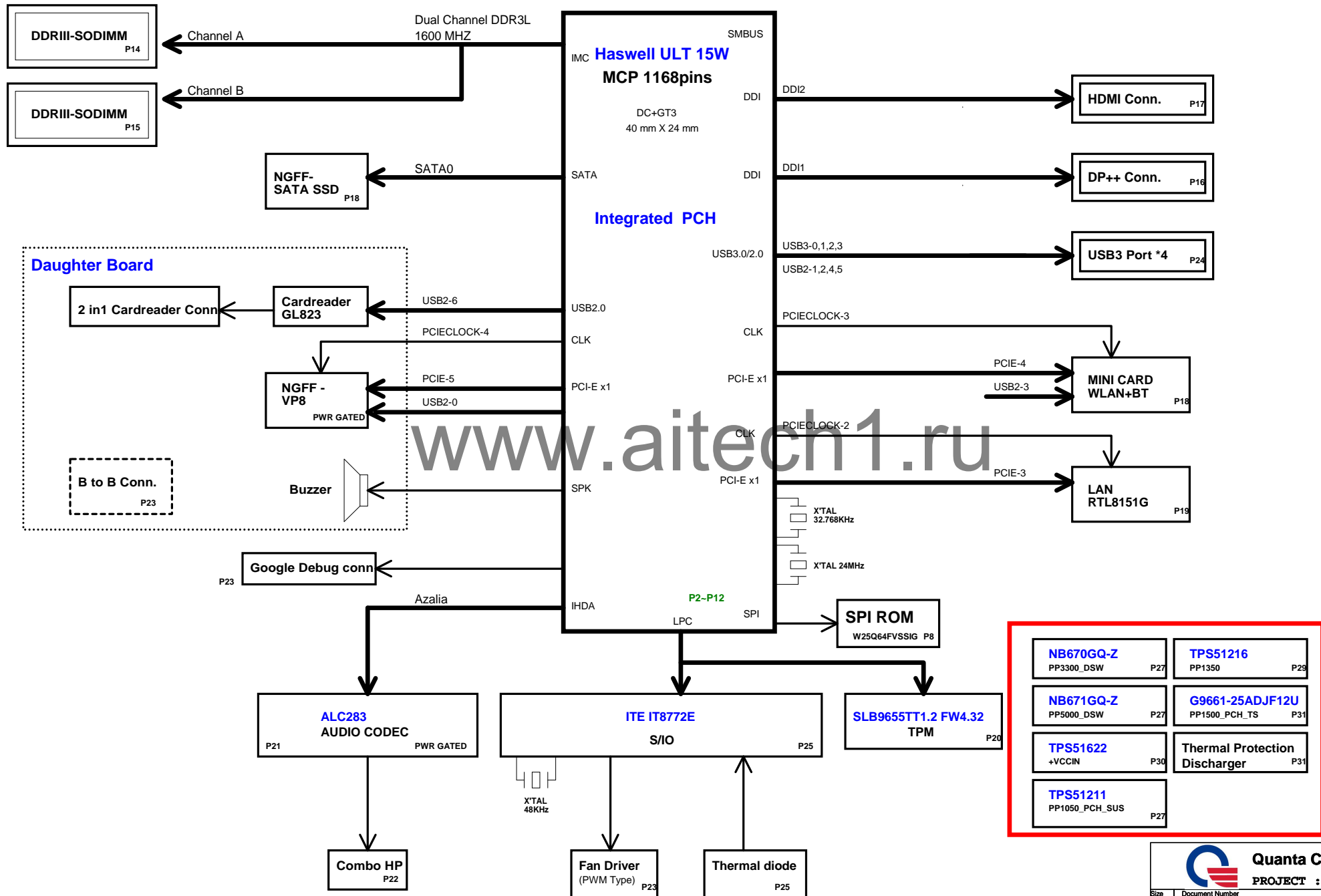
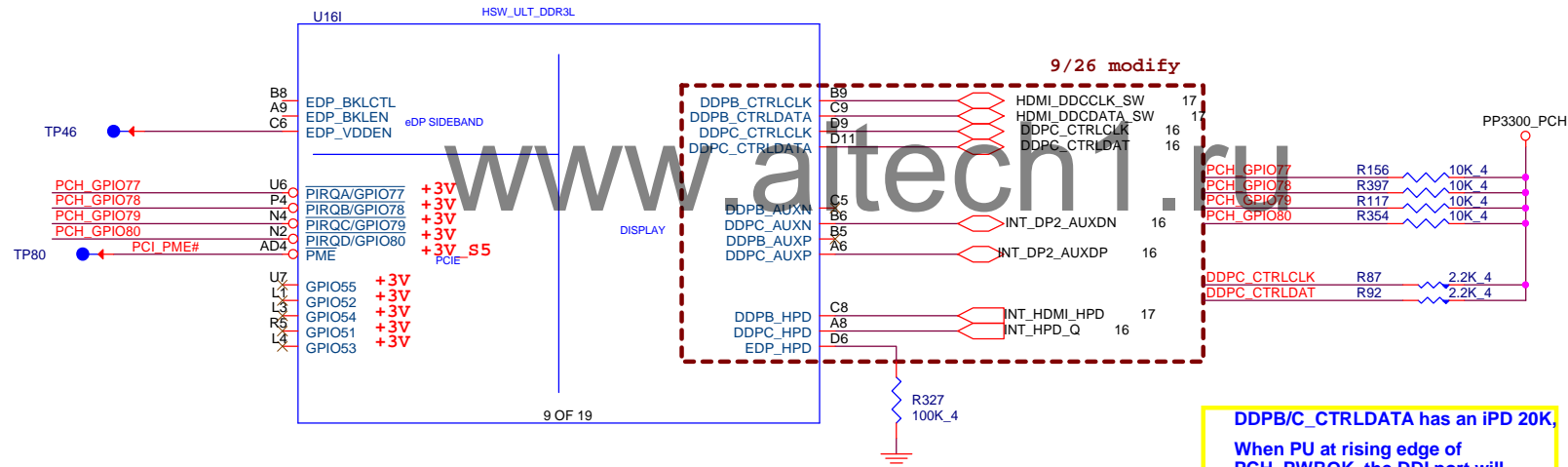
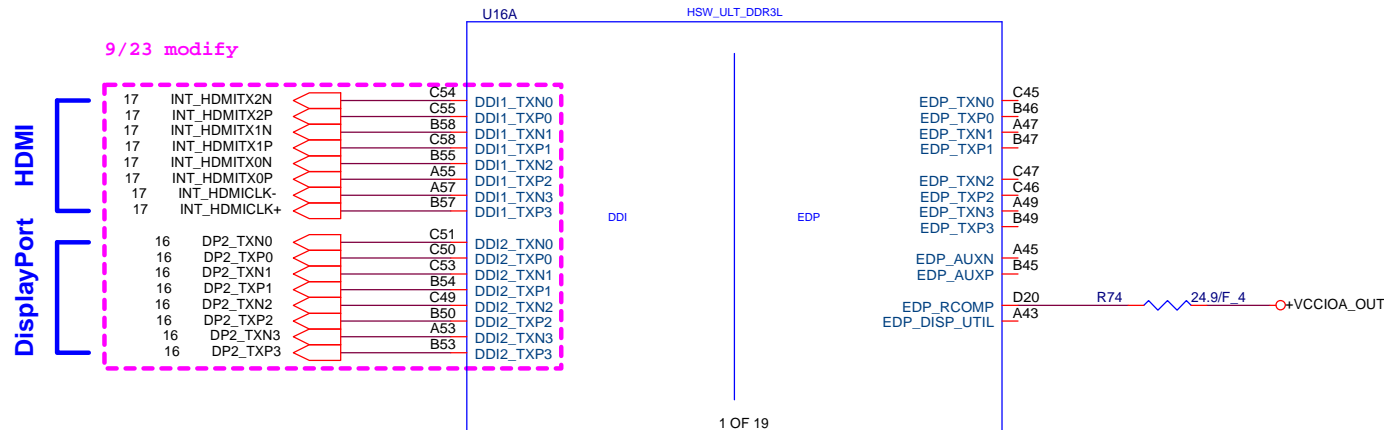


ZAKO/0W9 SHB ULT SYSTEM BLOCK DIAGRAM



Haswell ULT (DISPLAY,eDP)



Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

DDPB/C_CTRLCLK has an iPD 20K.
When PU at rising edge of PCH_PWROK, the DDI port will be detected

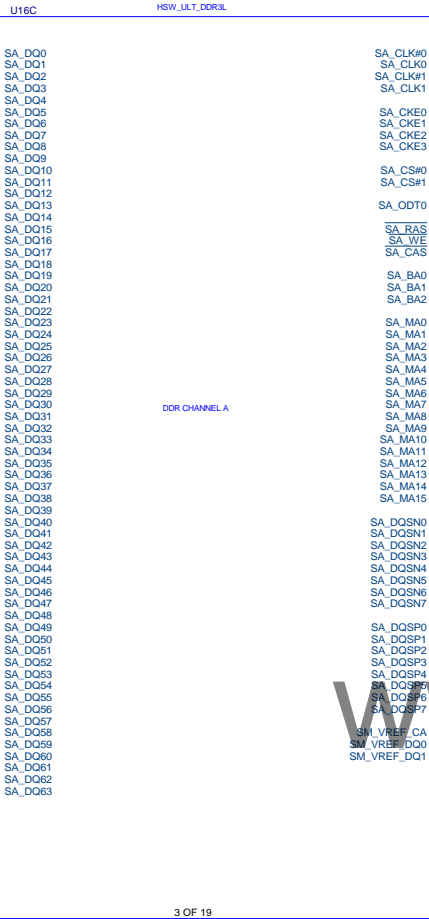


Quanta Computer Inc.

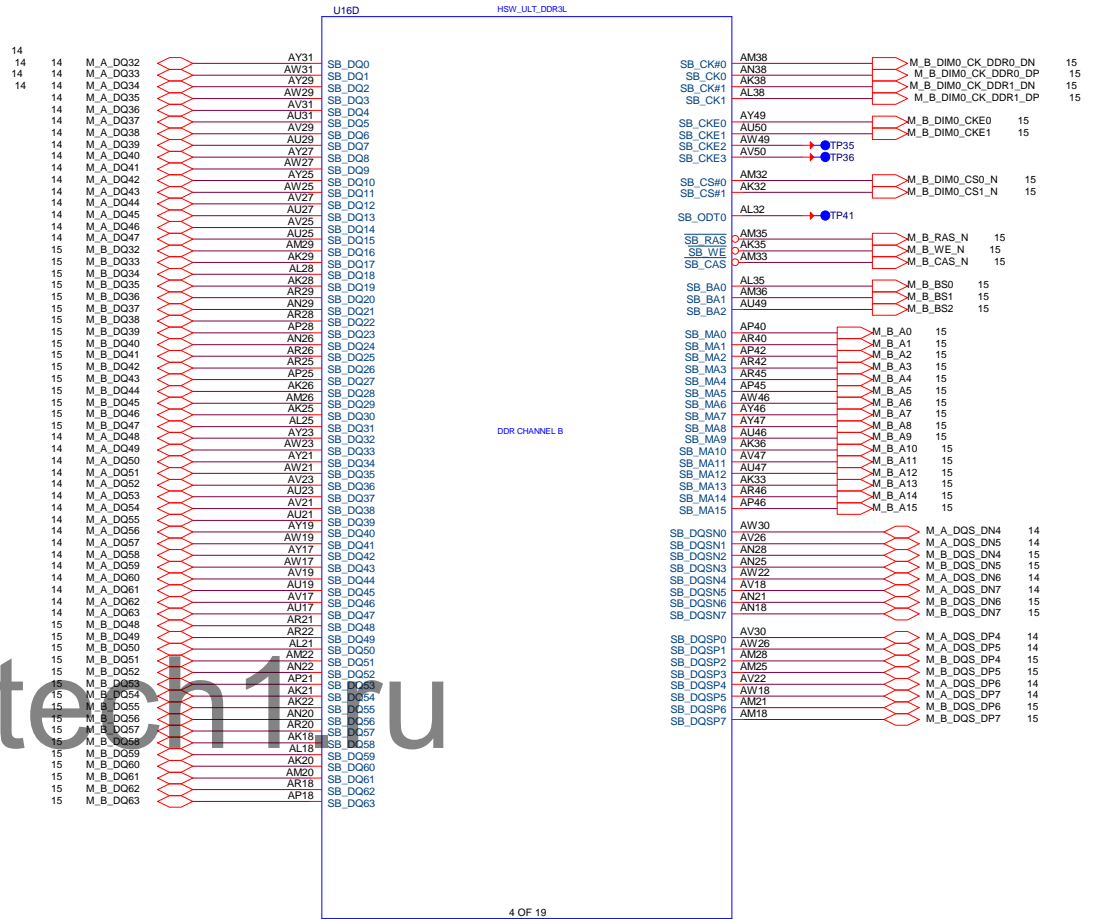
PROJECT : 0W9

Size	Document Number	Rev
	Haswell 1/5 (DDI/eDP)	3A
Date:	Monday, March 31, 2014	Sheet 2 of 33

Haswell ULT (DDR3L)



Haswell Processor (DDR3L)

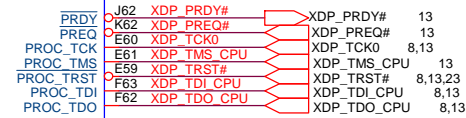
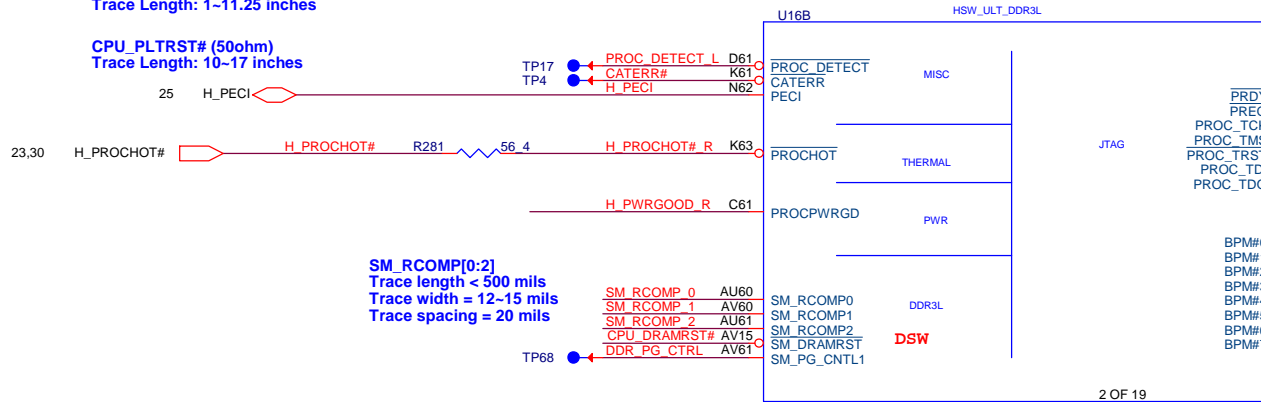


Haswell ULT (SIDE BAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

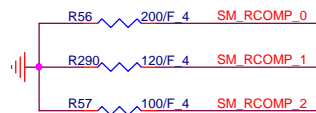
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



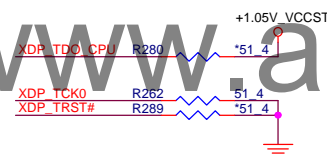
TCK, TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

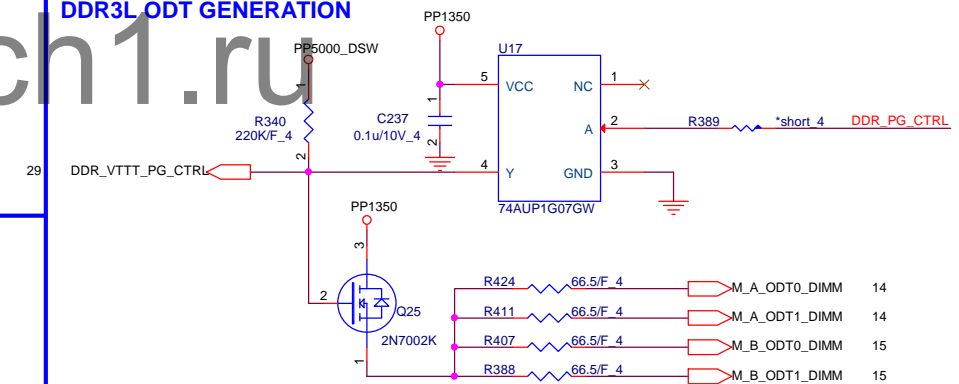
DRAM COMP



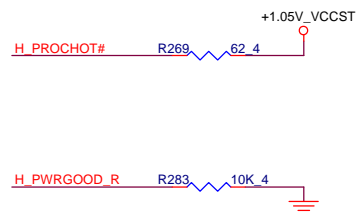
XDP PU/PD



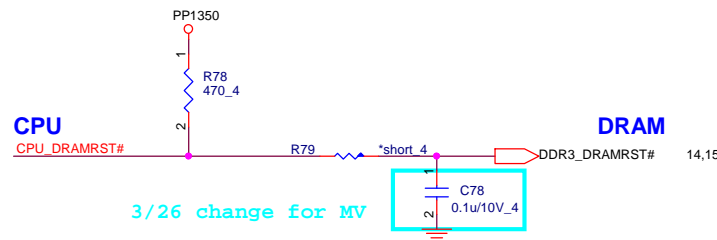
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST

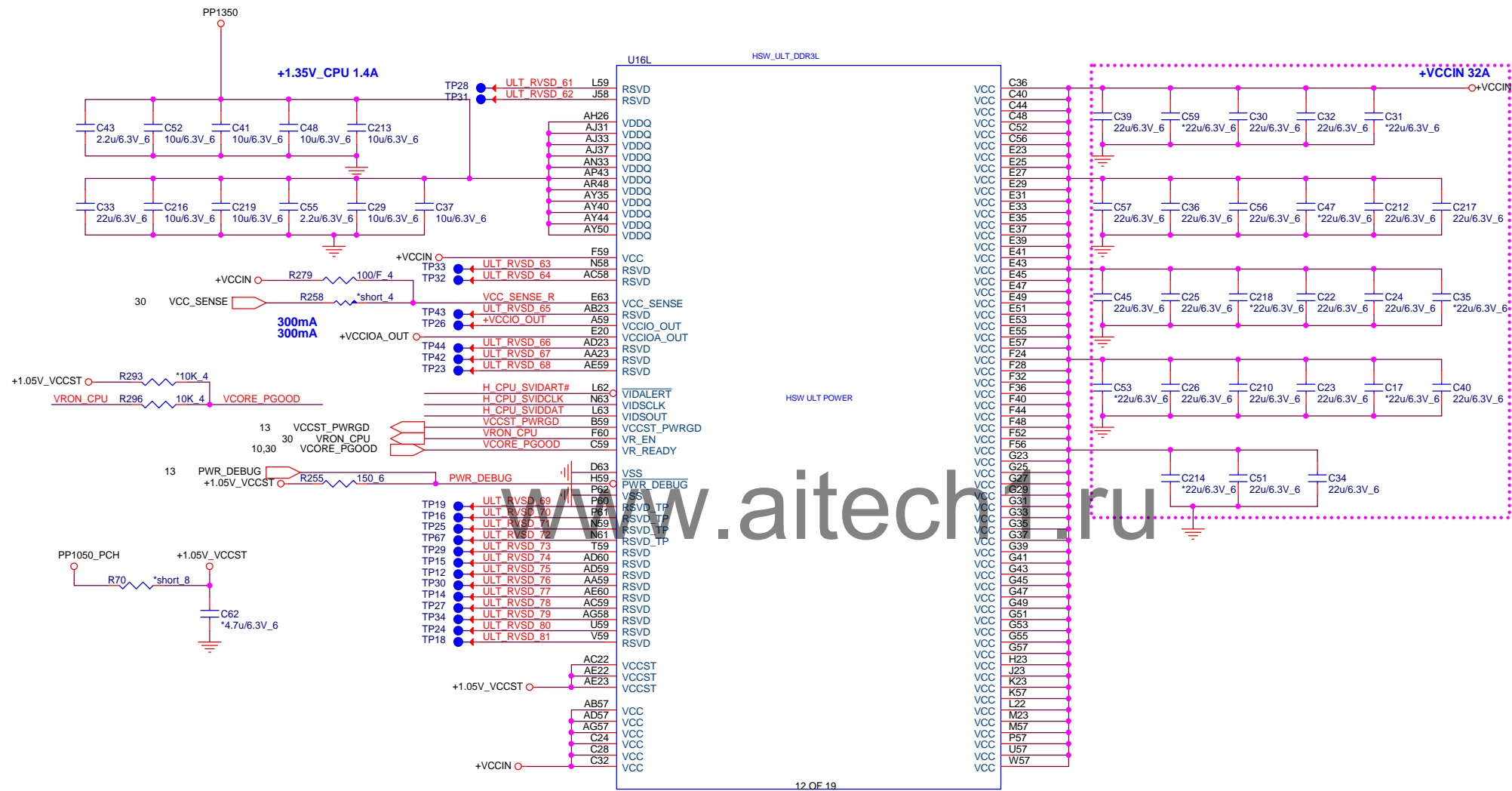


Quanta Computer Inc.

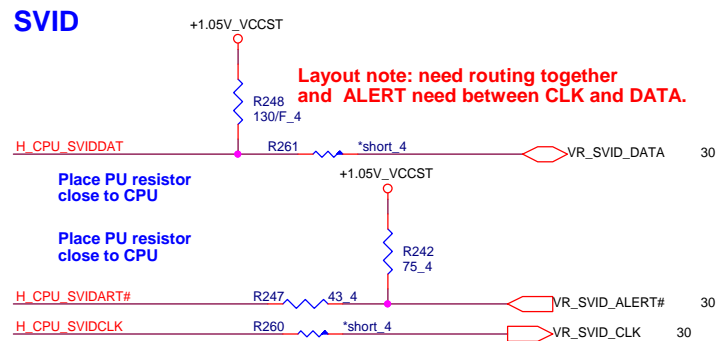
PROJECT : 0W9

Size	Document Number	Rev
	Haswell 3/5 (SideBand)	3A
Date:	Monday, March 31, 2014	Sheet 4 of 33

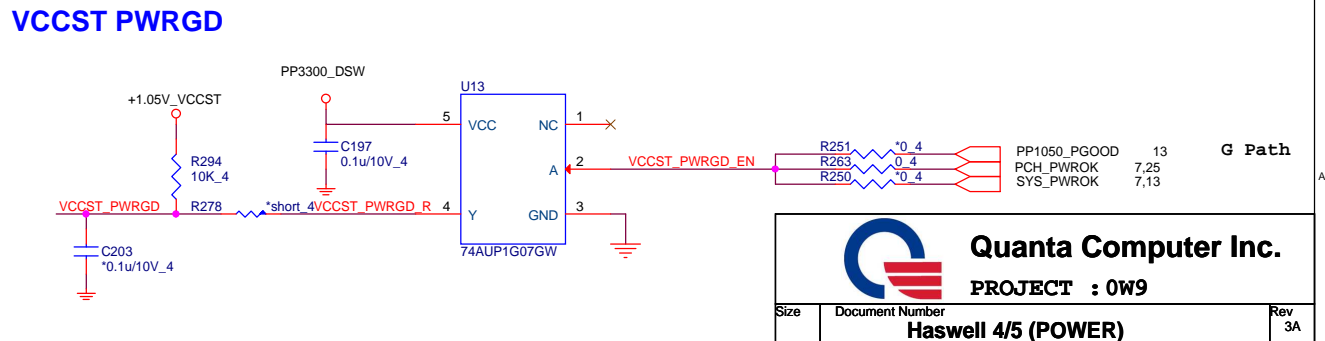
Haswell ULT (POWER)



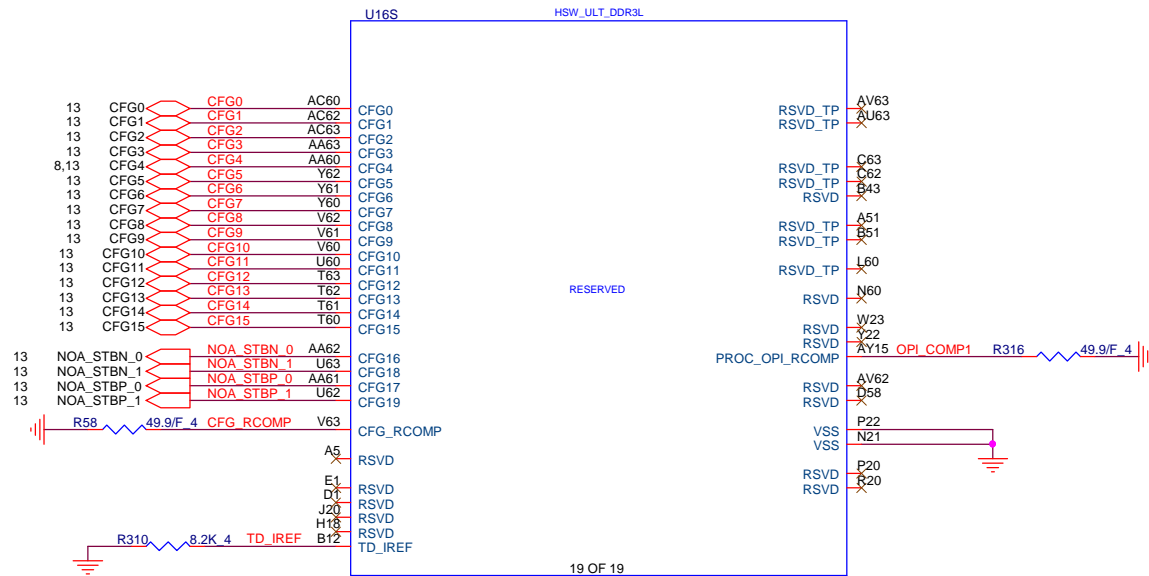
SVID



VCCST PWRGD



Haswell ULT (CFG,RSVD)



Processor Strapping

CFG0	1	0	
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R268 *1K 4
CFG1	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R264 *1K 4
CFG3	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R265 *1K 4
CFG 8	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R53 *1K 4
CFG9	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R54 *1K 4
CFG10	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATING) ARE NOT ACTIVATED	CFG10 R50 *1K 4



Quanta Computer Inc.
PROJECT : 0W9

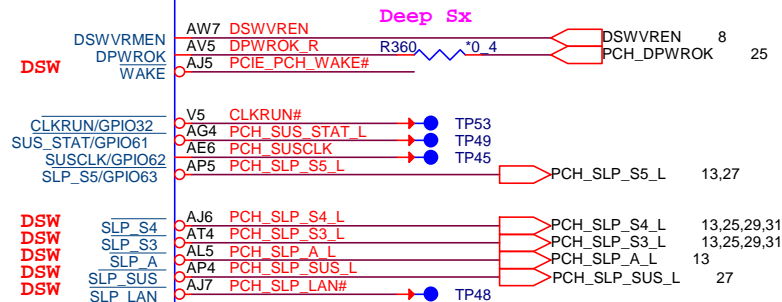
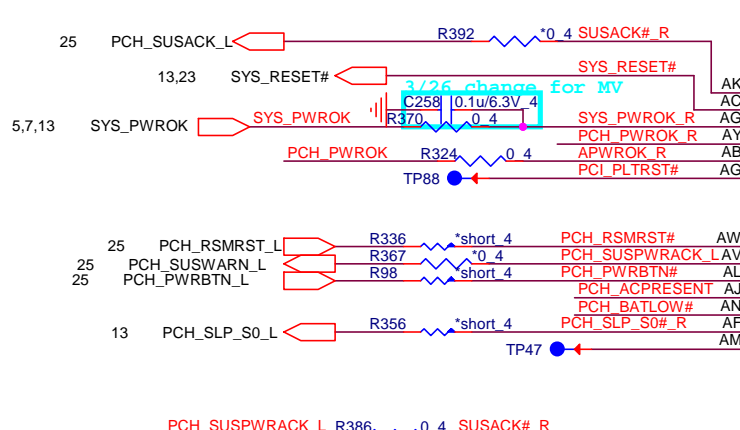
Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A
Date:	Monday, March 31, 2014	Sheet 6 of 33

IUH6

SYSTEM POWER MANAGEMENT

SUSACK			D5WVRMEN
SYS_RESET			DPWORH
SYS_PWROK		D5W	WAKEUP
PCH_PWROK			
APWROK			
PLTRST +3V_S5	+3V		
	+3V_S5		
	+3V_S5		
	D5W		
RSMRST			CLKRUN/GPIO32
SUSWARN/SUSPWRDNACK/GPIO30	+3V_S5		SUS_STAT/GPIO61
			SUSCLK/GPIO6
			SLP_S5/GPIO63
PWRBTN	D5W	D5W	
ACPRESENT/GPIO31	D5W	D5W	SLP_S4
BATLOW/GPIO72	D5W	D5W	SLP_S3
SLP_S0	+3V_S5	D5W	SLP_A
SLP_WLAN/GPIO29	D5W	D5W	SLP_SUS
			SLP_LAN

8 OF 19



The schematic diagram illustrates the PP3300 power plane, which is connected to the PCH (Platform Controller Hub) and DSX (Data Switching) components. The power plane is represented by a central horizontal line with various signals and resistors connected to it.

PP3300_PCH Connections:

- CLKRUN#** (R119) is connected to the power plane with a value of $\sim 8.2K$ 4.
- SYS_RESET#** (R368) is connected to the power plane with a value of $10K$ 4.
- PCH_RSMRST#** (R337) is connected to the power plane with a value of $10K$ 4.
- SYS_PWROK** (R404) is connected to the power plane with a value of $\sim 10K$ 4.
- DPWROK_R** (R363) is connected to the power plane with a value of $100K/F$ 4.
- CLKRUN#** (R507) is connected to the power plane with a value of 0 4.

PP3300_PCH_SUS Connections:

- PCH_SUSPWRACK_L** (R364) is connected to the power plane with a value of $10K$ 4.

PP3300_DSX Connections:

- PCH_ACPRESENT** (R150) is connected to the power plane with a value of $10K$ 4.
- PCH_BATLOW#** (R371) is connected to the power plane with a value of $8.2K$ 4.
- PCIE_PCH_WAKE#** (R127) is connected to the power plane with a value of $10K$ 4.
- PCH_PWRBTN#** (R95) is connected to the power plane with a value of $\sim 10K$ 4.

PLTRST# Buffer

PCI_PLTRST# R165 *short PLTRST#

PP3300_PCH

C118 *0.1u/10V 4

5

2

1

PCI_PLTRST#

4

PLTRST# 13,18,19,20,23,25

U5 *TC7SH08FU

3

R178 100K_4

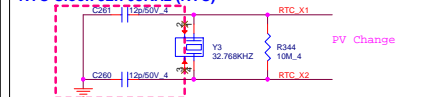
```
graph LR
    PP3300_PCH --- R165 --- PCI_PLTRST#
    PP3300_PCH --- C118 --- GND
    PP3300_PCH --- U5_2[U5 Pin 2]
    PCI_PLTRST# --- U5_1[U5 Pin 1]
    U5_1 --- U5_3[U5 Pin 3]
    U5_3 --- GND
    U5_3 --- U5_4[U5 Pin 4]
    U5_4 --- R178 --- GND
    U5_4 --- PLTRST#
    PLTRST# --- Pins[13,18,19,20,23,25]
```



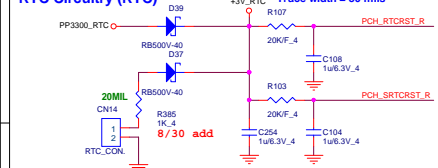
PROJECT : 0W9

Size	Document Number PCH 1/6 (PM)	Rev 3A
Date:	Monday, March 31, 2014	Sheet 7 of 33

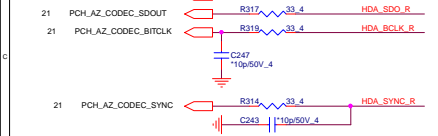
RTC Clock 32.768KHz (RTC)



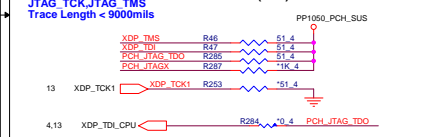
RTC Circuitry (RTC)



HDA



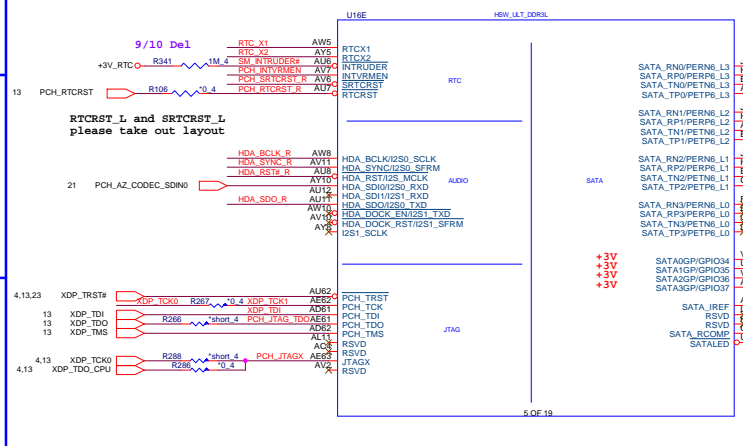
PCH JTAG



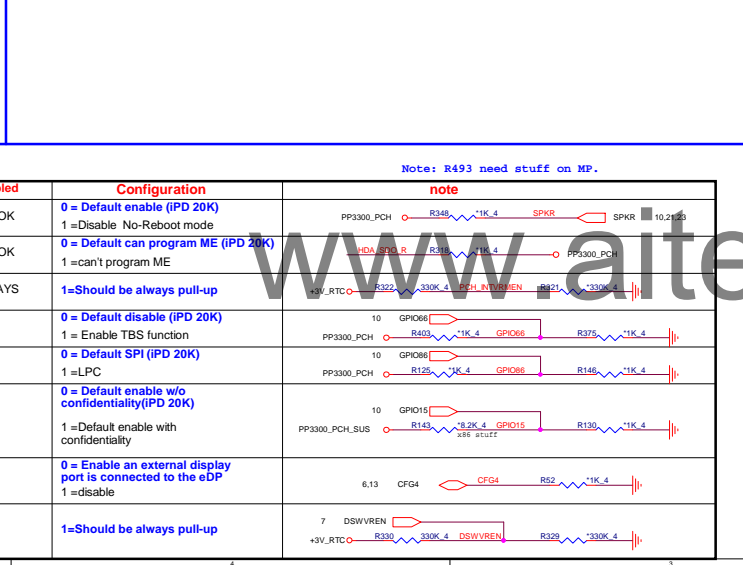
ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (IPD 20K) 1 = can't program ME
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up
GPIO66	Top-Block Swap override		0 = Default disable (IPD 20K) 1 = Enable TBS function
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(IPD 20K) 1 = Default enable with confidentiality
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable
DSWVREN	Deep Sx well on the VR enable		1=Should be always pull-up

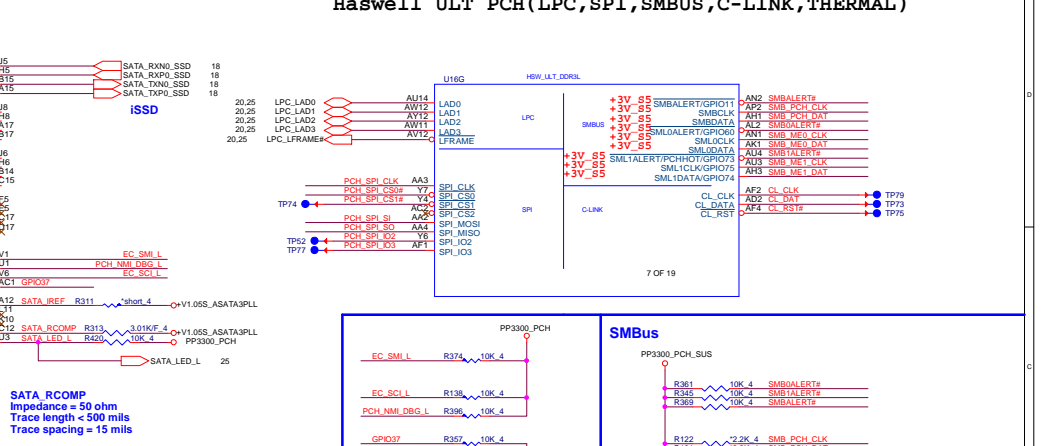
Haswell ULT PCH (RTC/HDA/SATA/SPI)



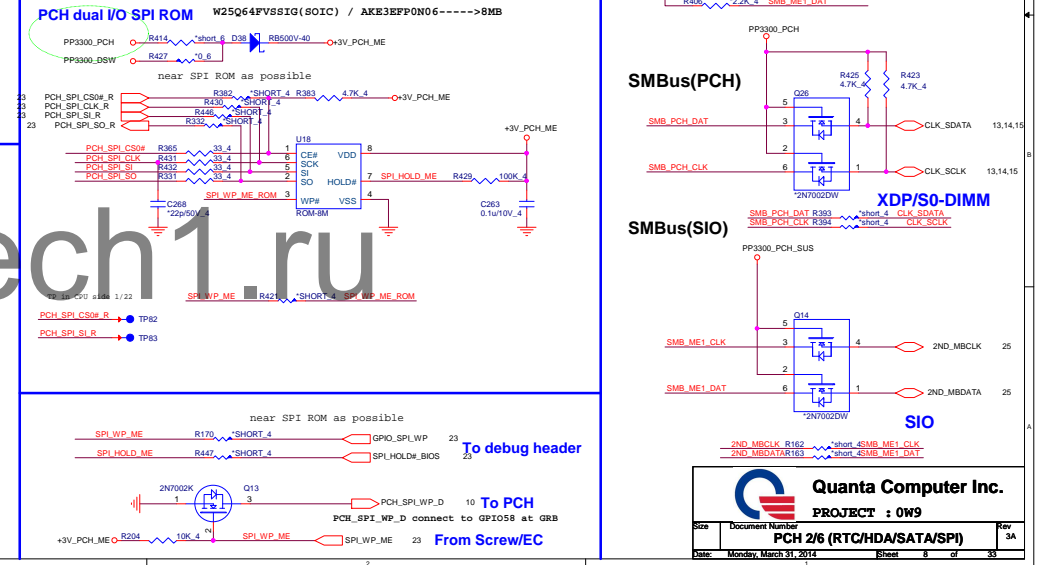
Haswell ULT PCH (LPC, SPI, SMBUS, C-LINK, THERMAL)



Haswell ULT PCH (LPC, SPI, SMBUS, C-LINK, THERMAL)



PCH dual I/O SPI ROM



SMBus(PCH)



SMBus(SIO)



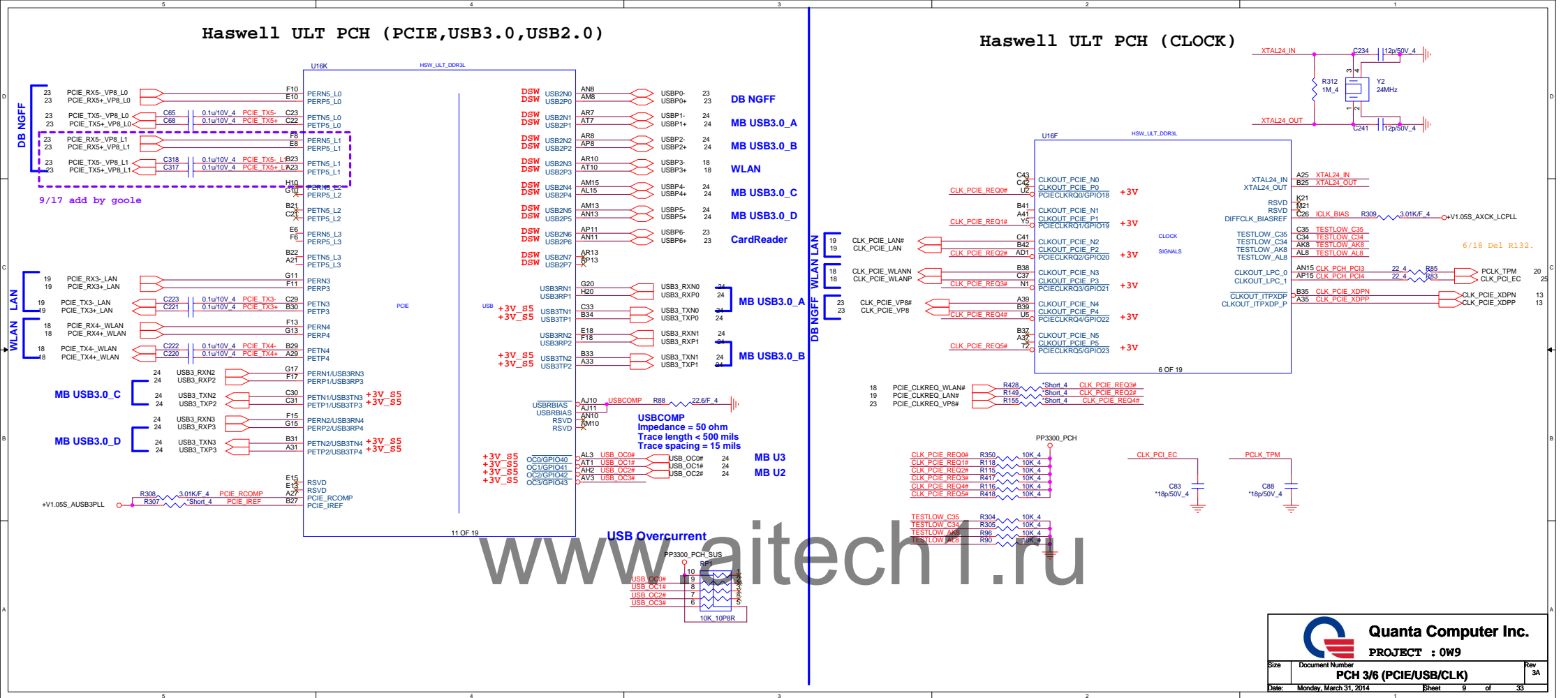
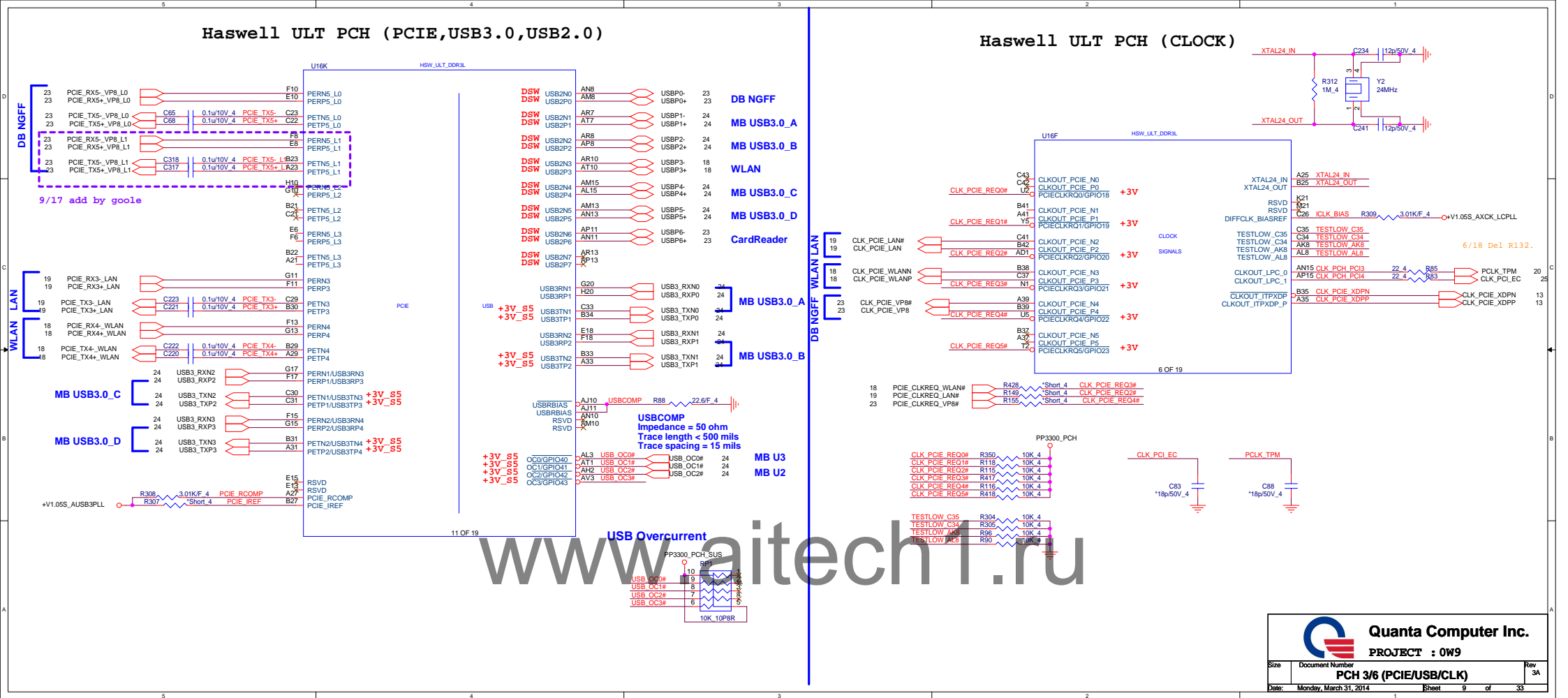
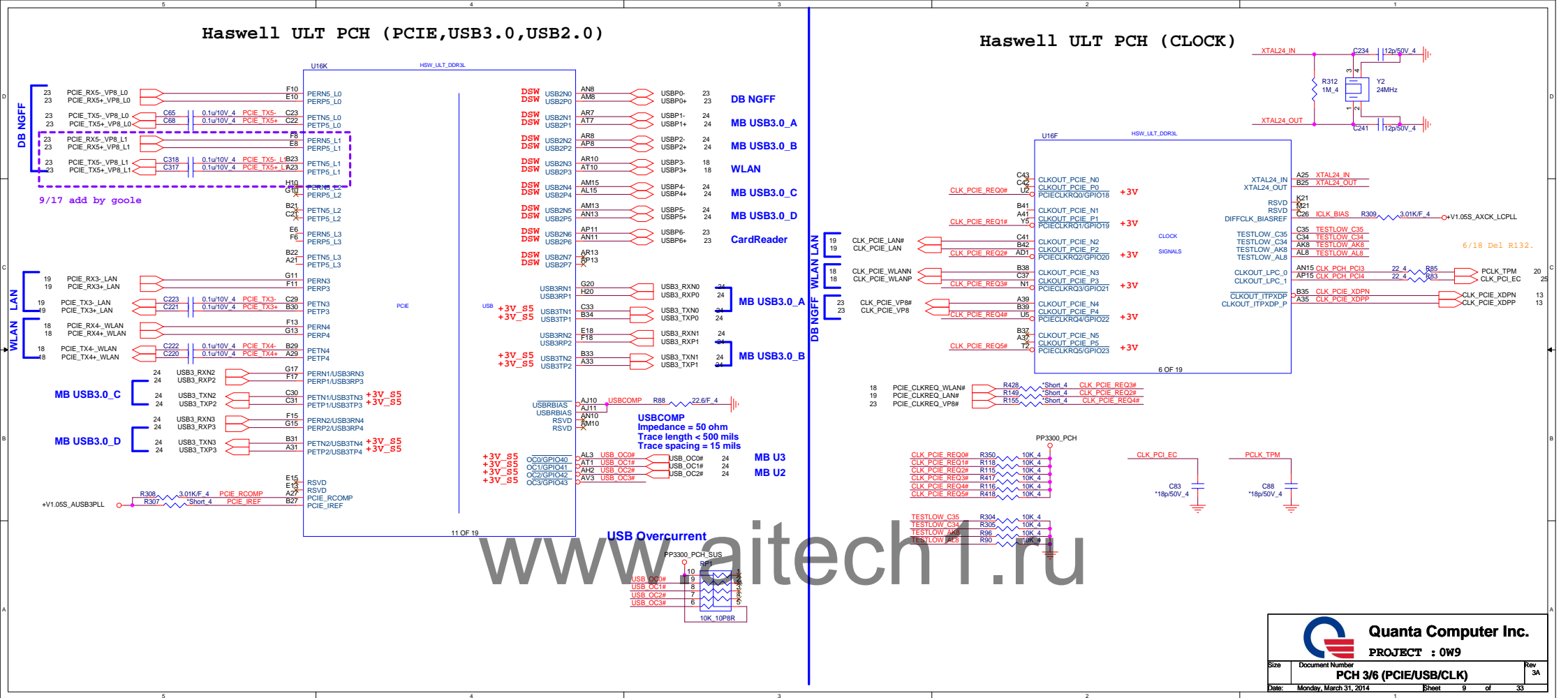
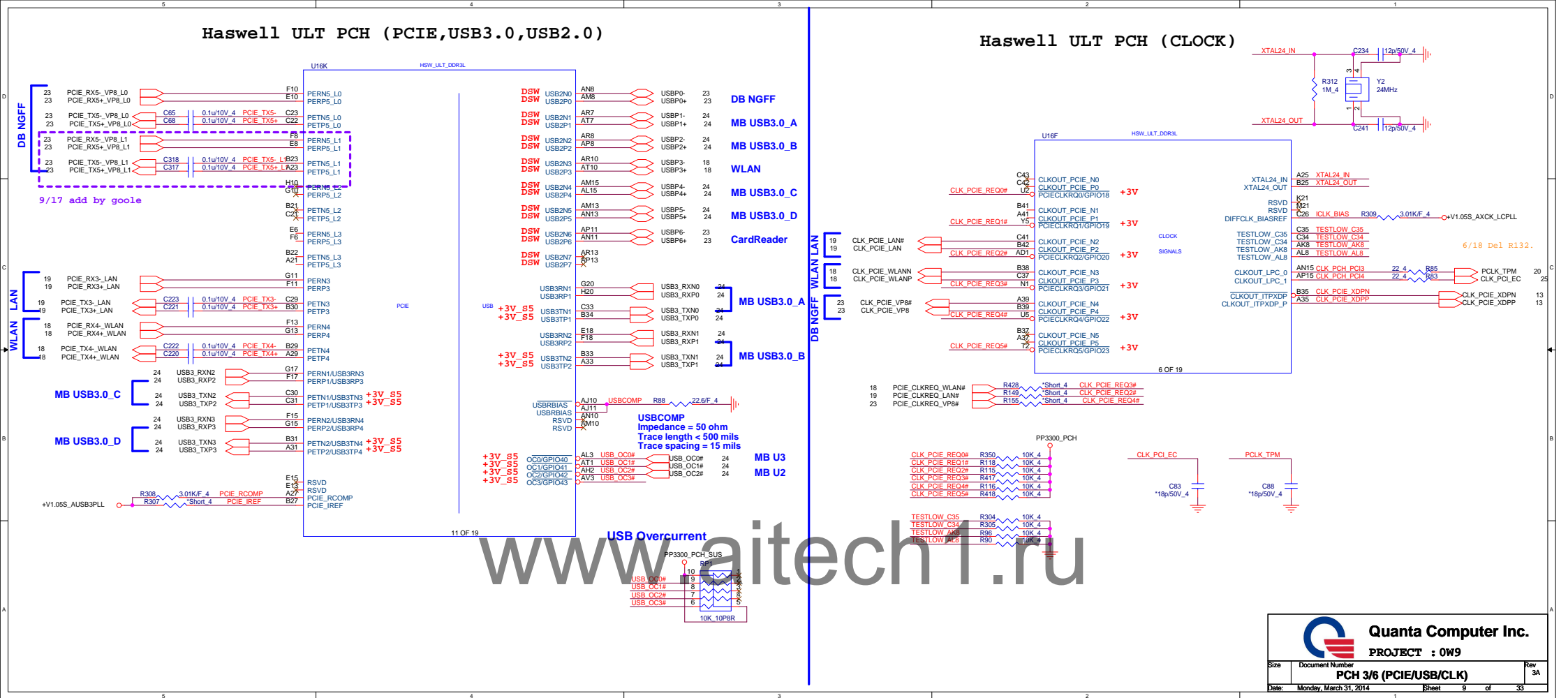
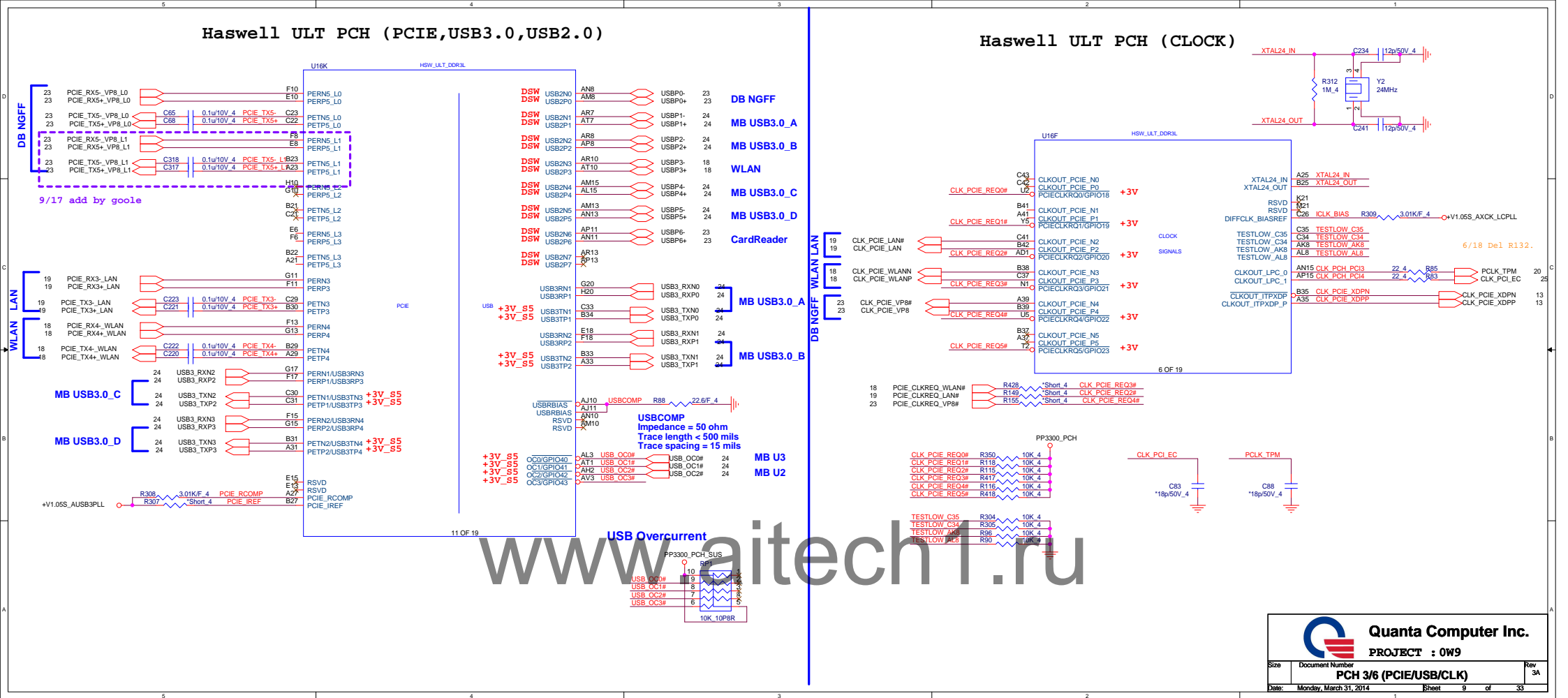
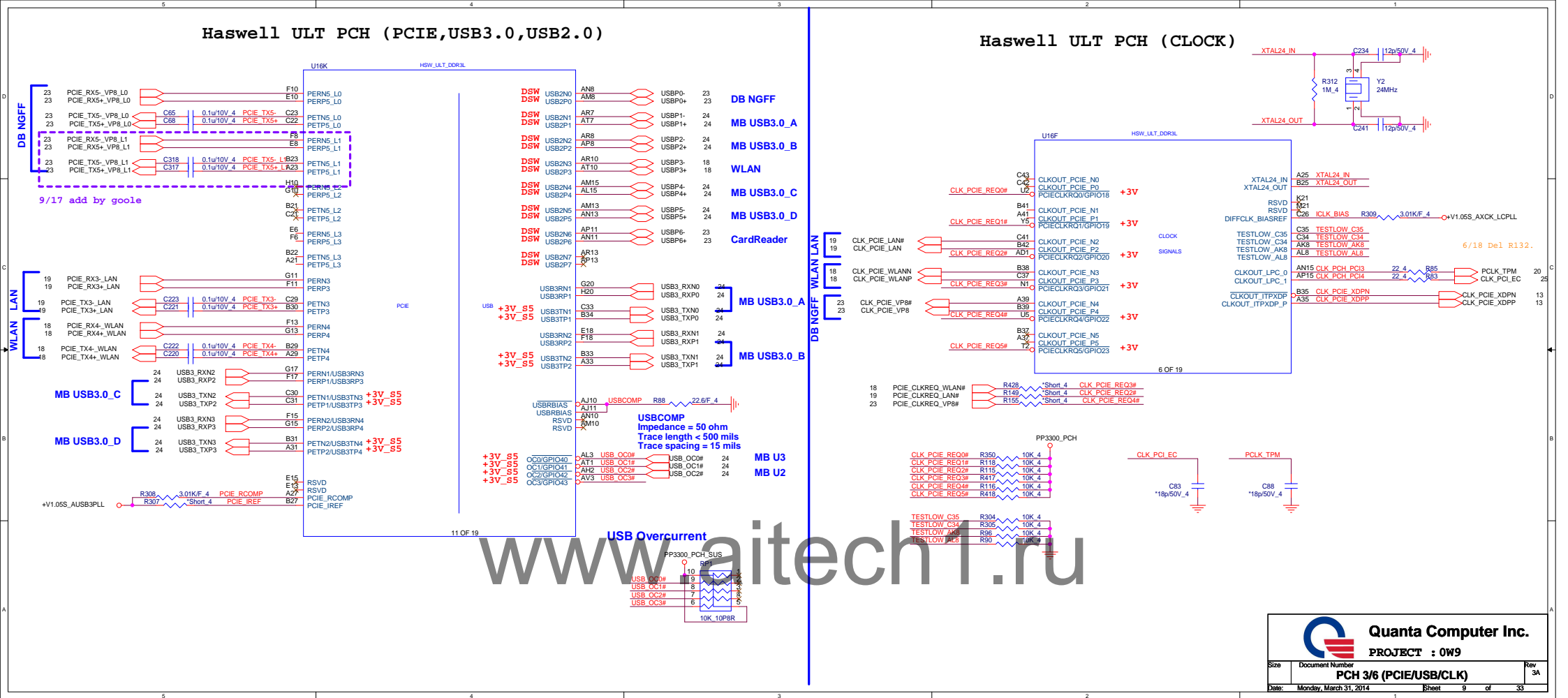
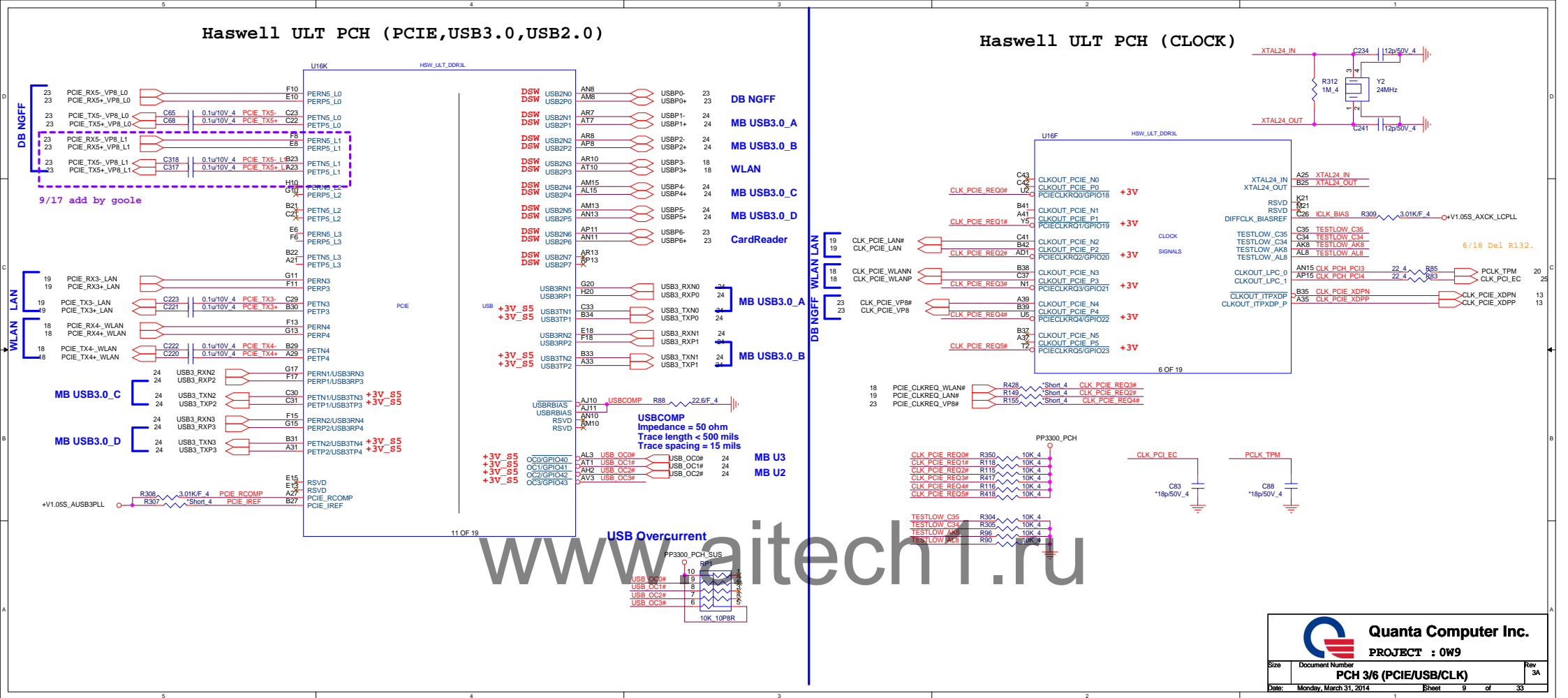
SIO



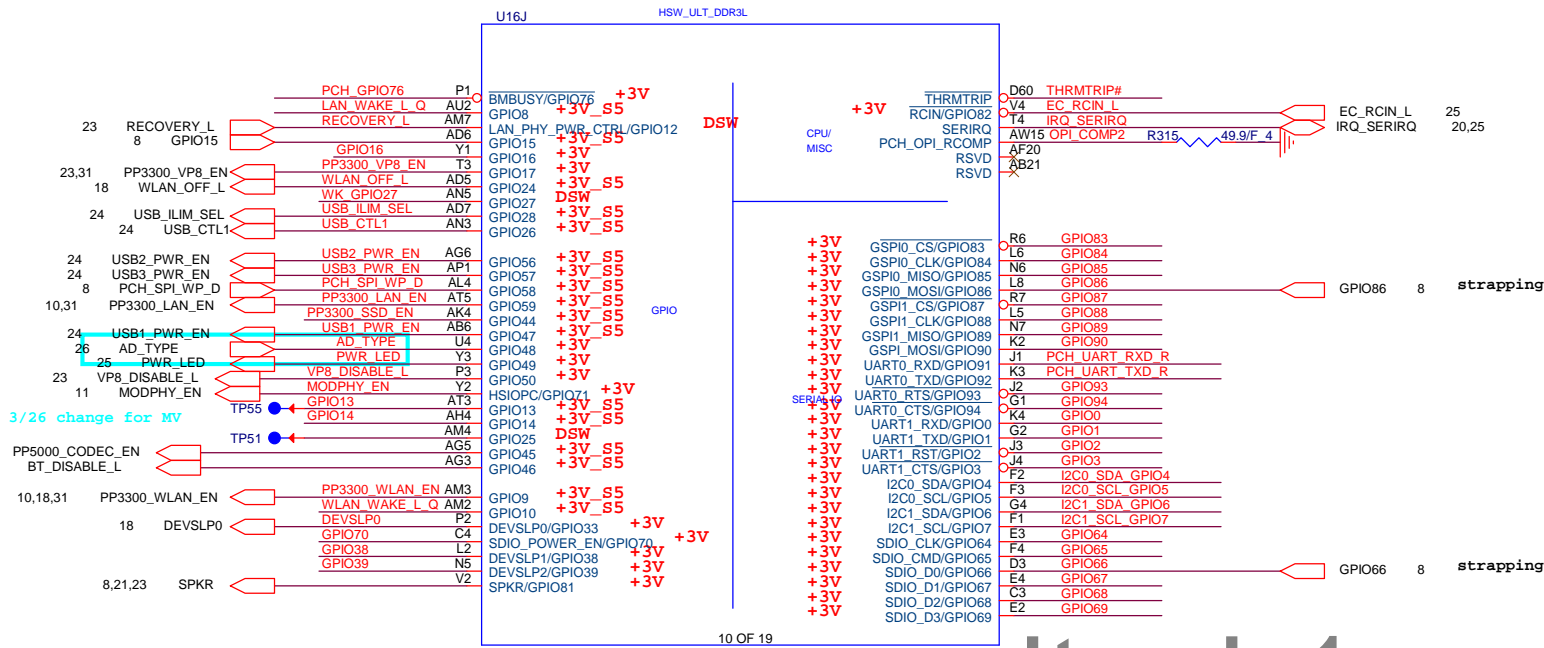
Quanta Computer Inc.

PROJECT : 0W9
PCH 2/6 (RTC/HDA/SATA/SPI)
Date: Monday, March 31, 2014 Sheet 8 of 30

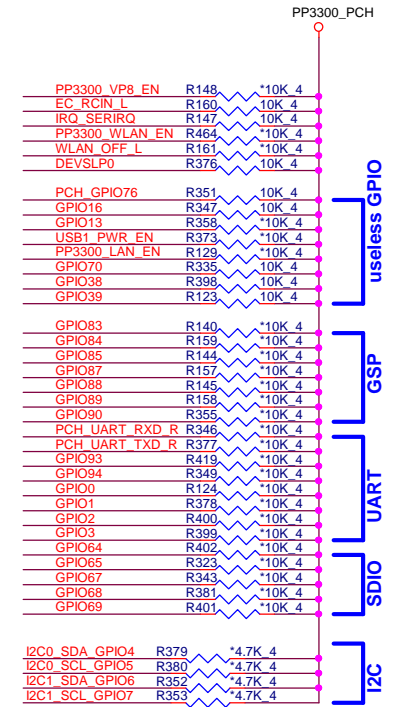
The image displays two PCB layout sheets for a Haswell ULT PCH (PCIE, USB3.0, USB2.0) and Haswell ULT PCH (CLOCK). The layout includes various components like resistors, capacitors, and connectors, with labels for DB NGFF, MB USB3.0 A, MB USB3.0 B, MB USB3.0 C, MB USB3.0 D, CardReader, MB USB3.0 A, MB USB3.0 B, MB U3, MB U2, and USB Overcurrent. It also shows a large watermark 'www.aitech1.ru'.



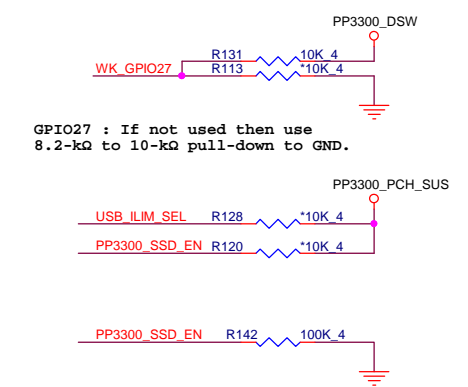
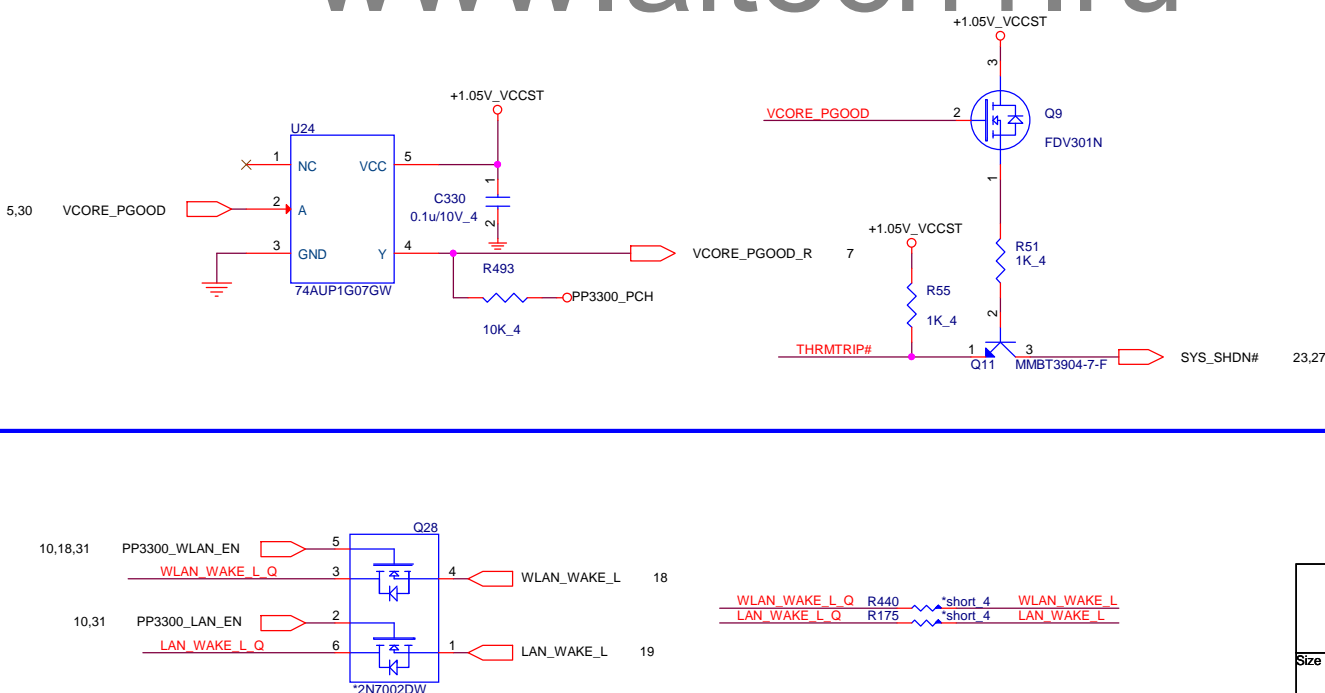
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

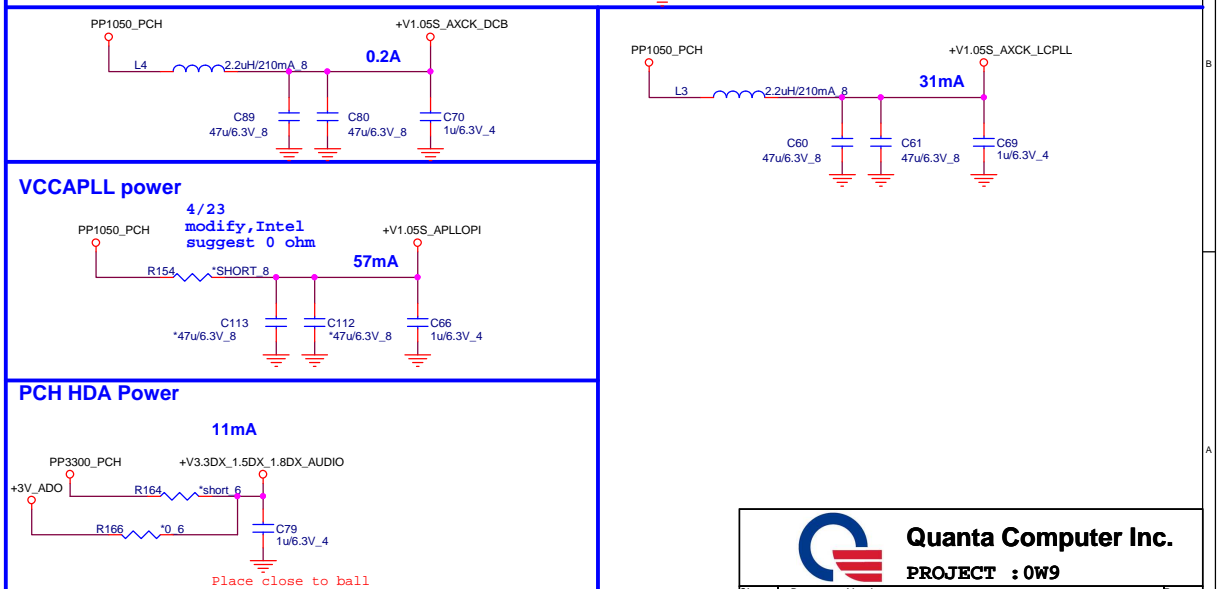
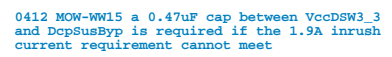


PCH GPIO PU/PD

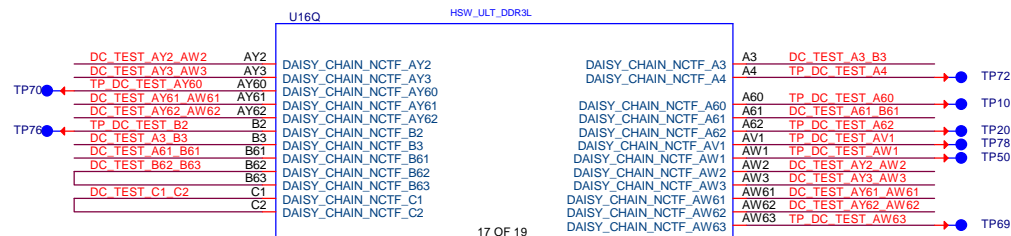
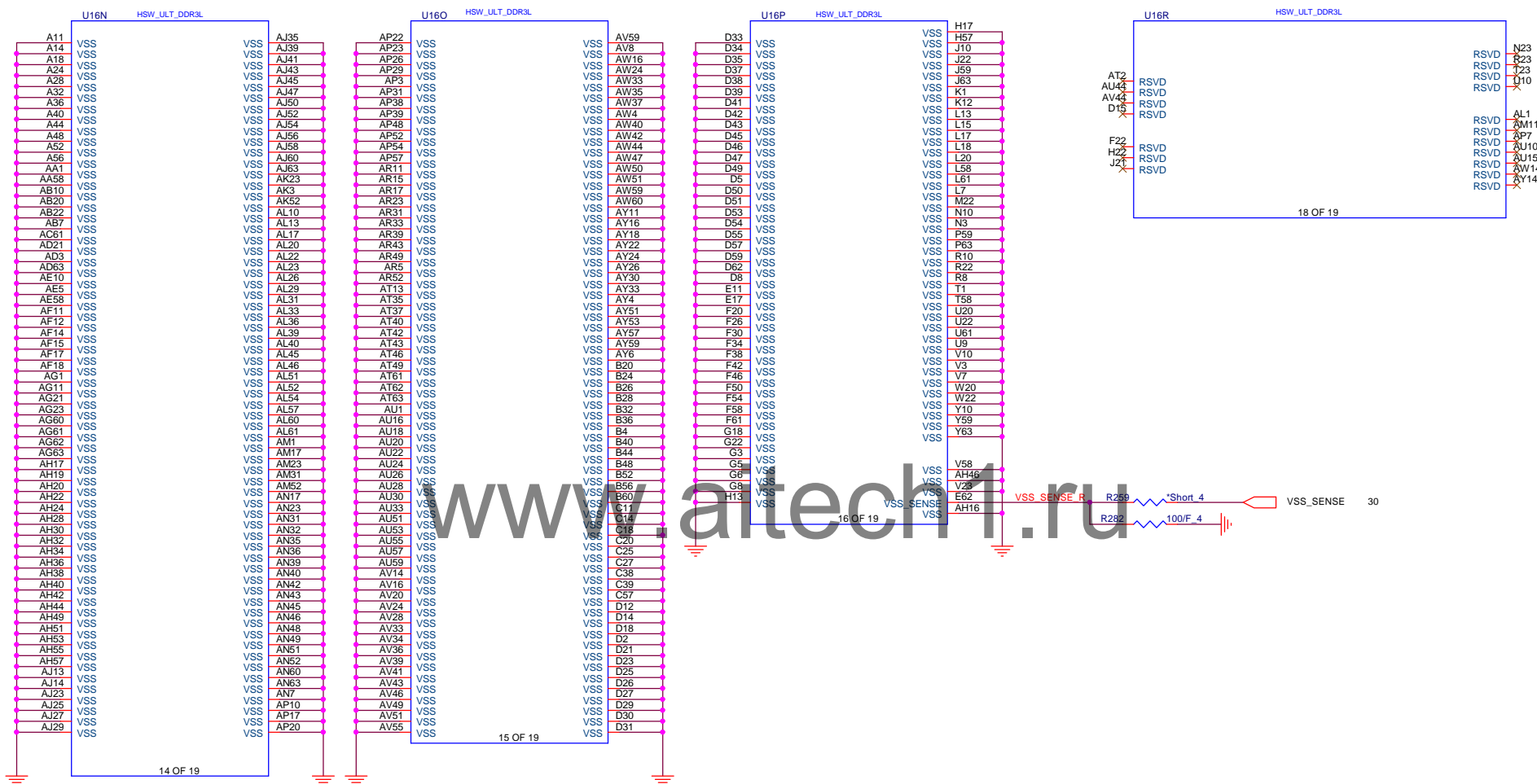


CPU thermal trip

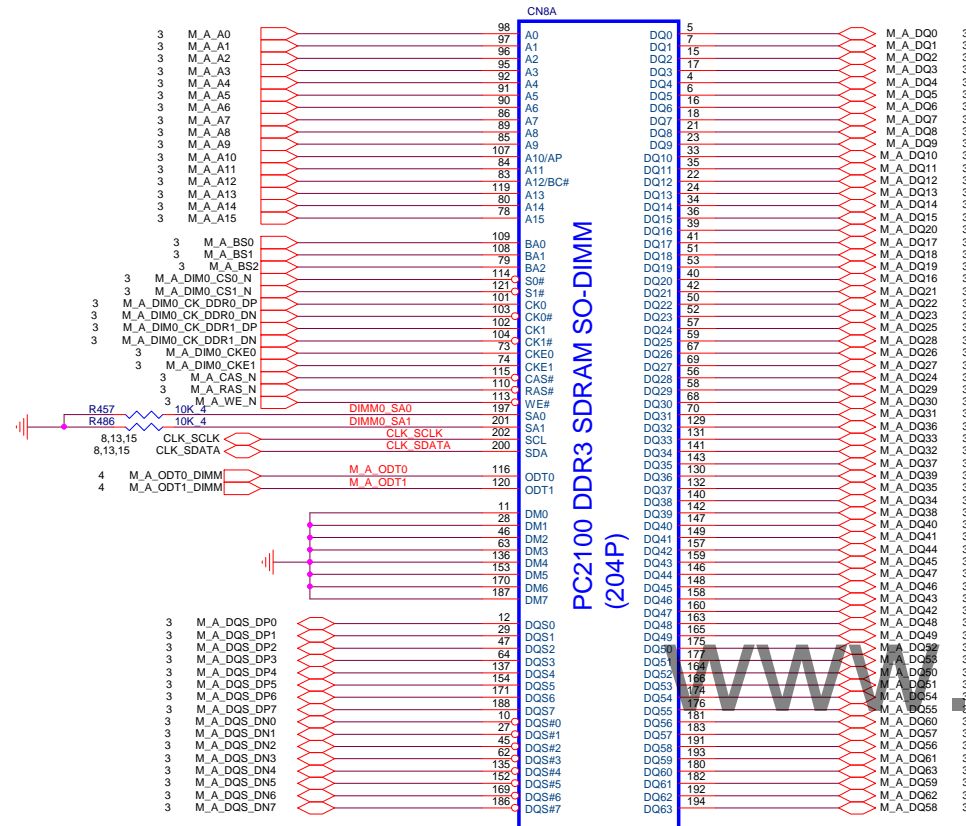




Haswell ULT (GND)



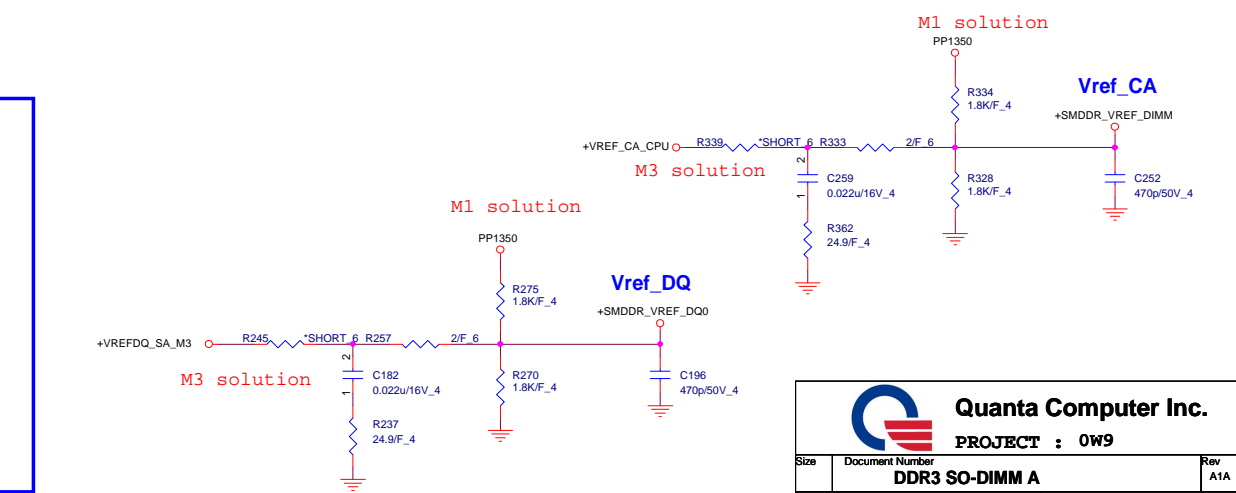
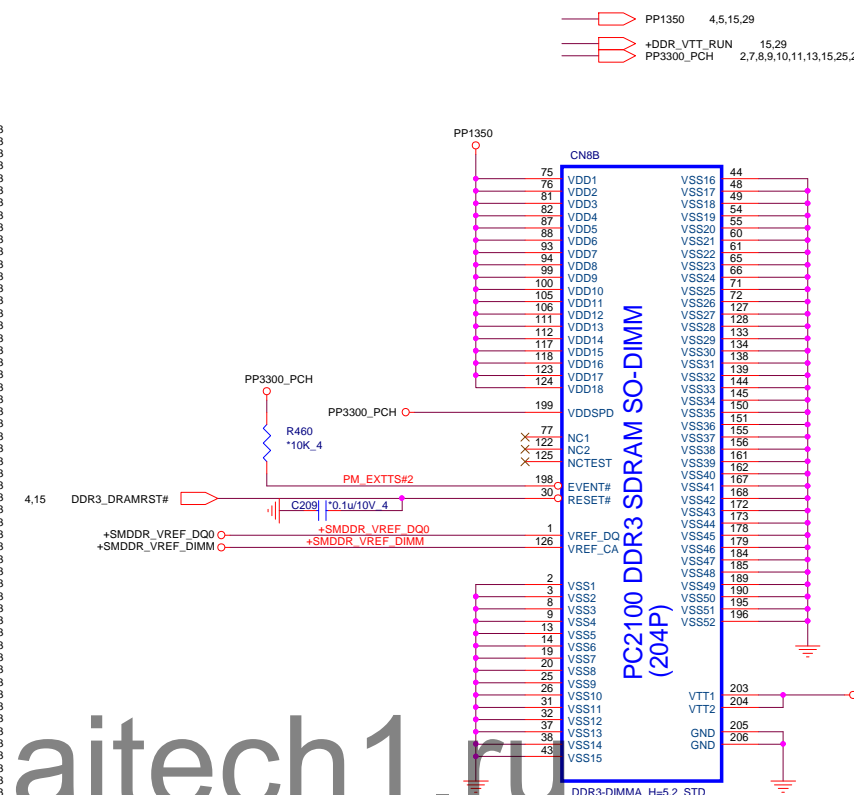
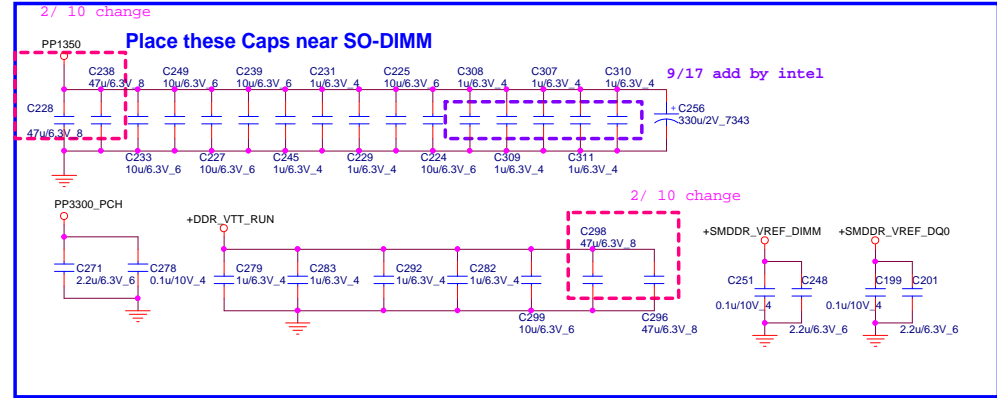
DDR3 DIMM-A



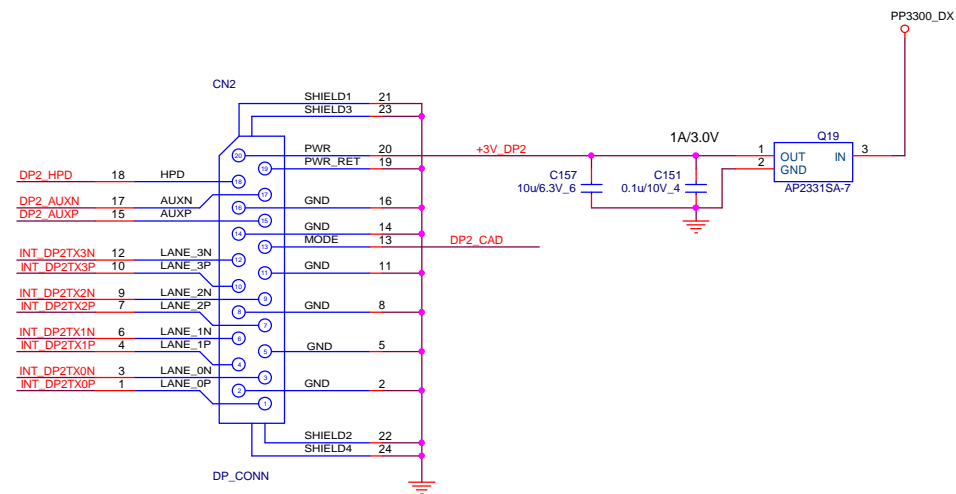
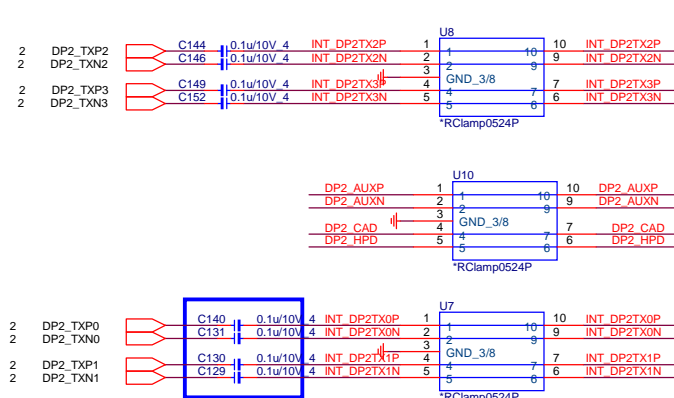
DDR3-DIMMA_H=5.2_STD

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

Place these Caps near So-Dimm A



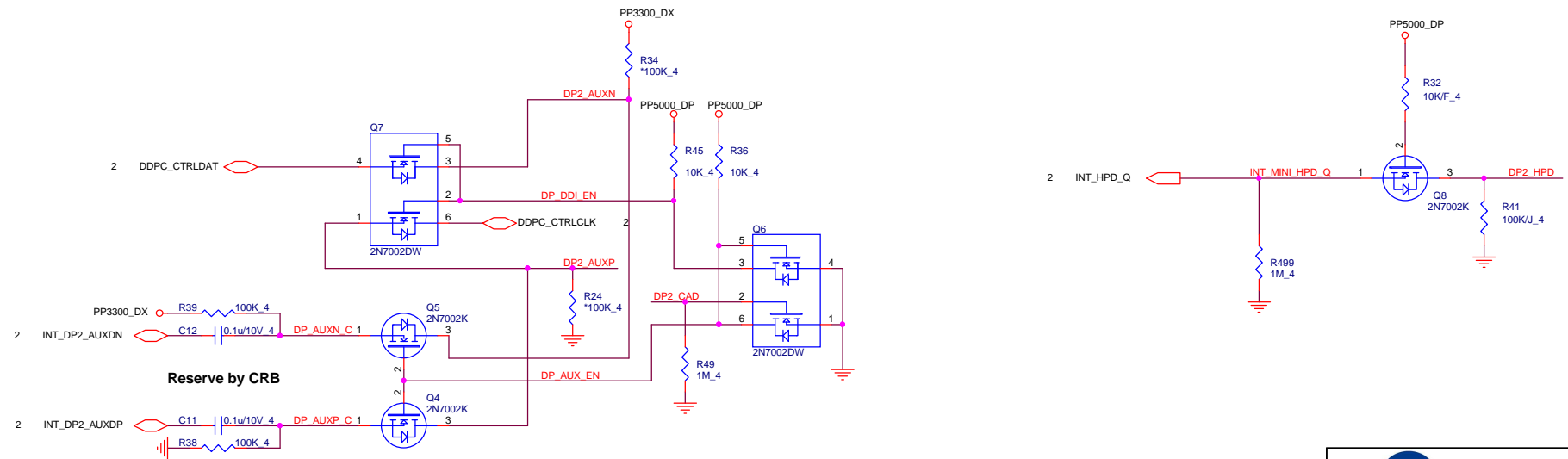
DisplayPort (DPP)



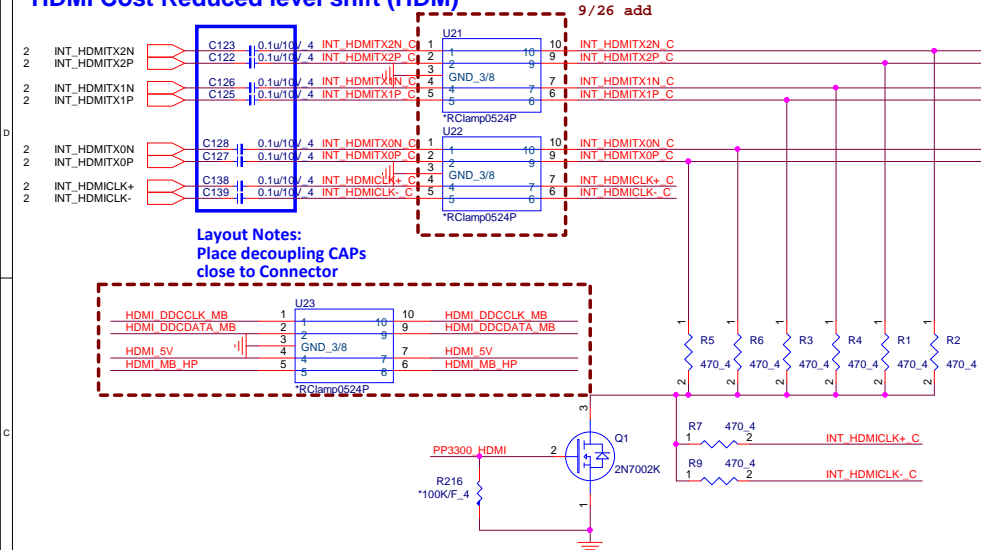
DP2 AUX (DPP)

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

www.aitech1.ru

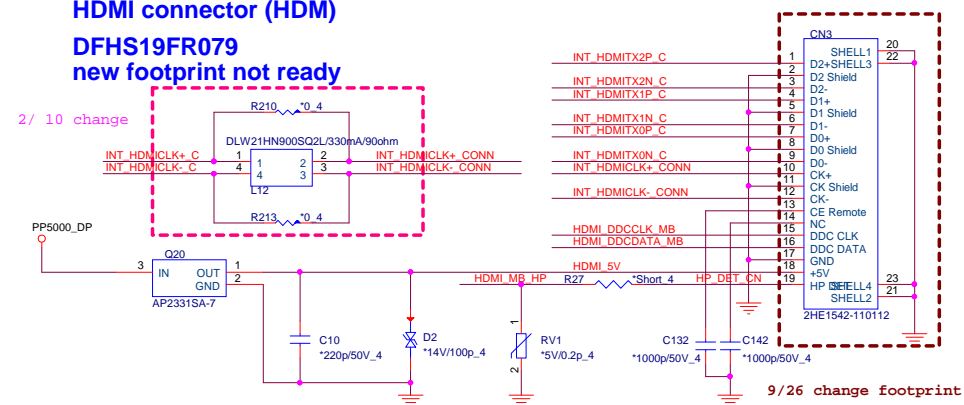


HDMI Cost Reduced level shift (HDM)

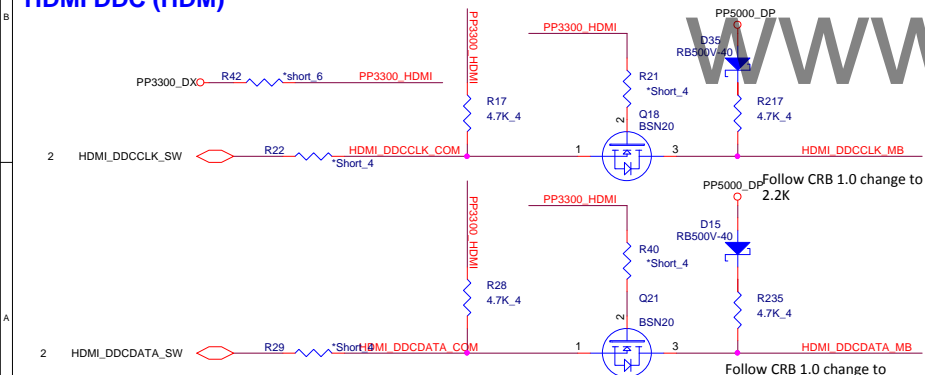


HDMI connector (HDM)

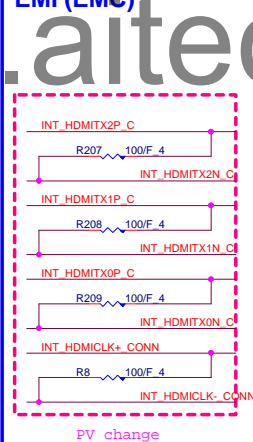
DFHS19FR079
new footprint not ready



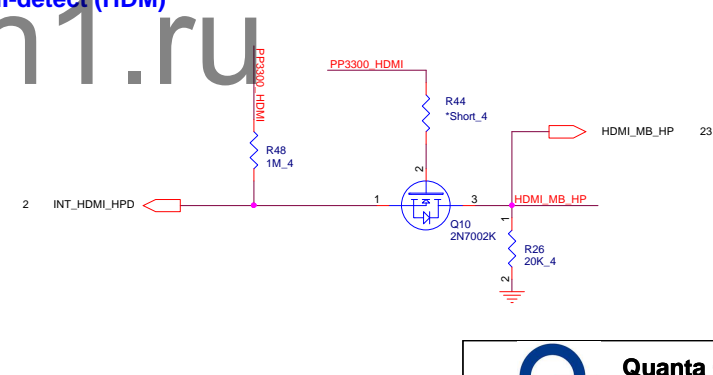
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)

**Quanta Computer Inc.**

PROJECT : 0W9

HDMI

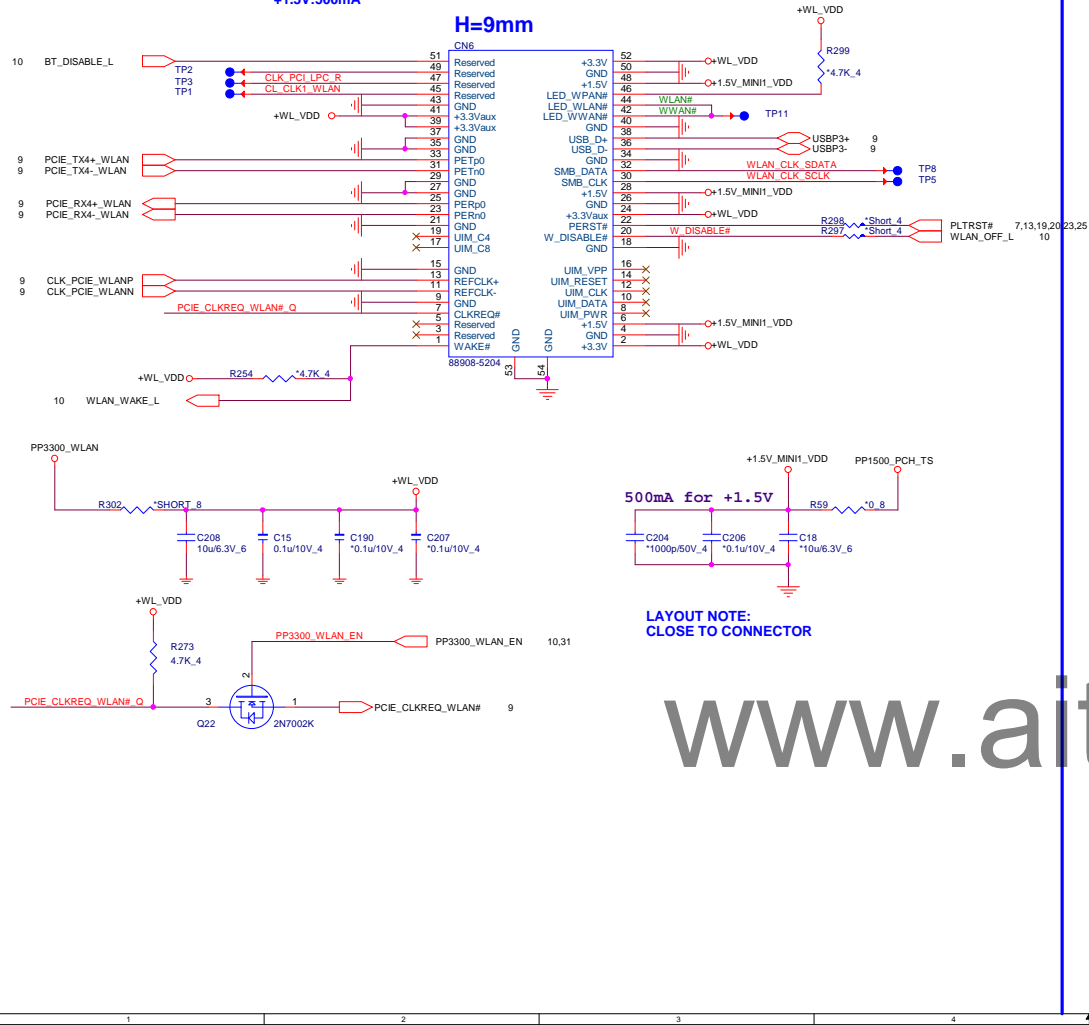
Rev
3A

Size	Document Number
Date:	Monday, March 31, 2014

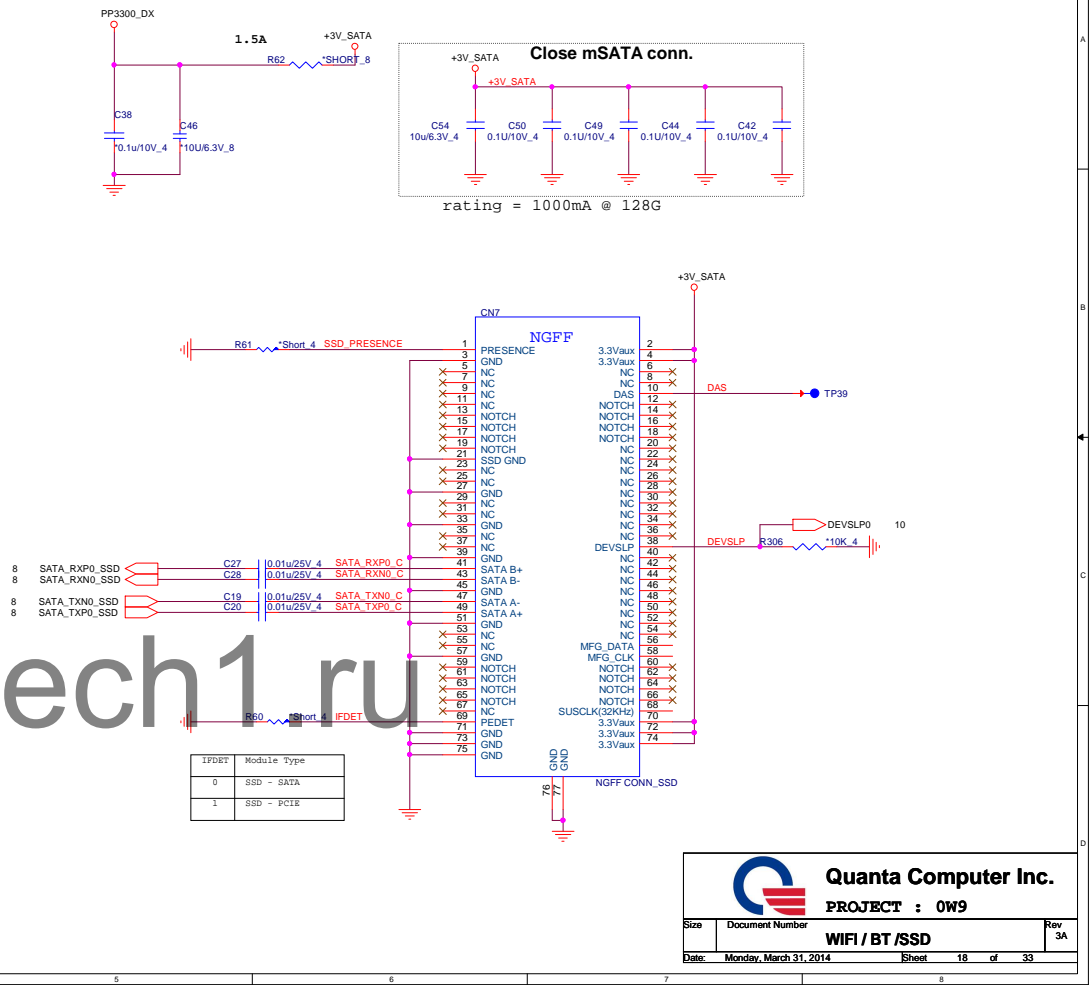
Sheet 17 of 33

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



NGFF SSD connector.



D

C

LAN PWR

B

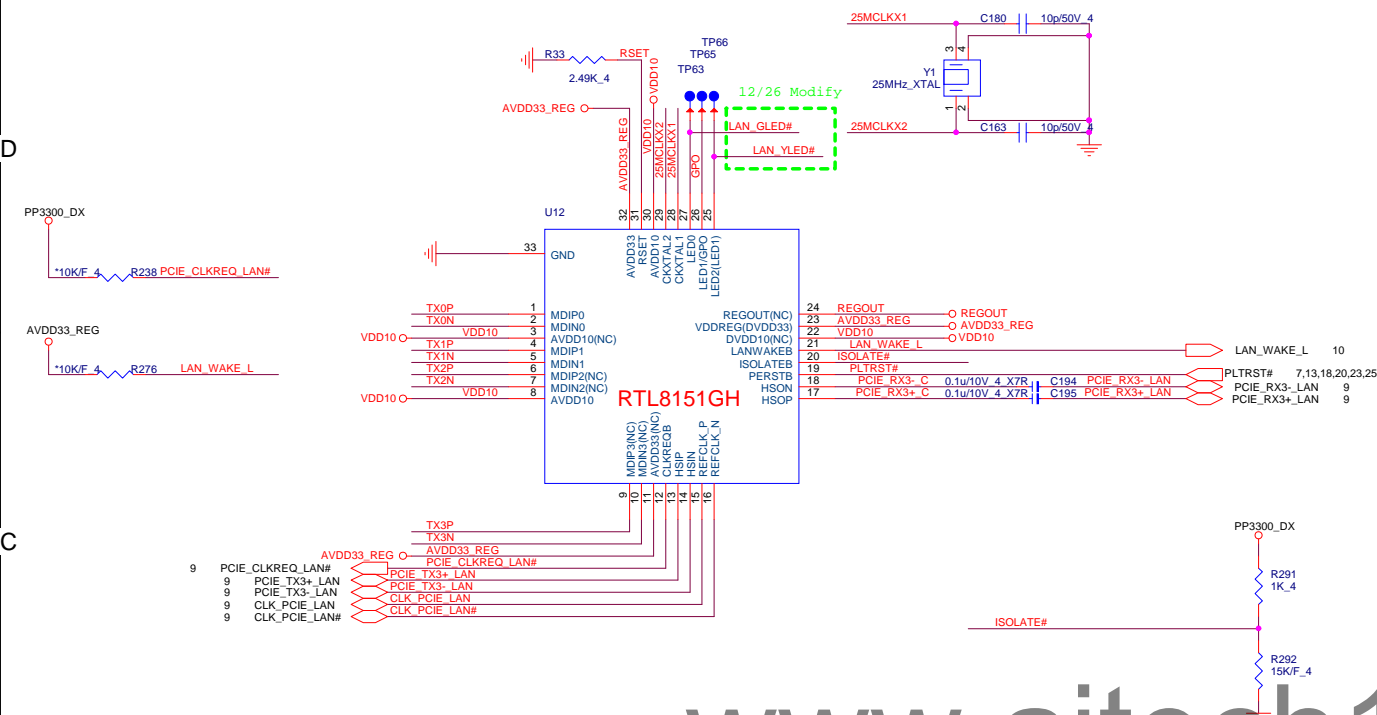
A

D

C

B

A

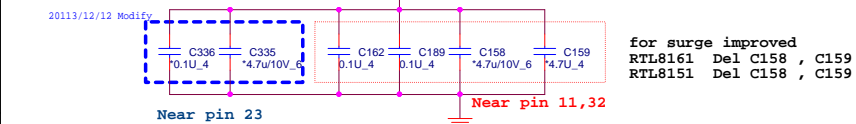


www.aitech1.ru

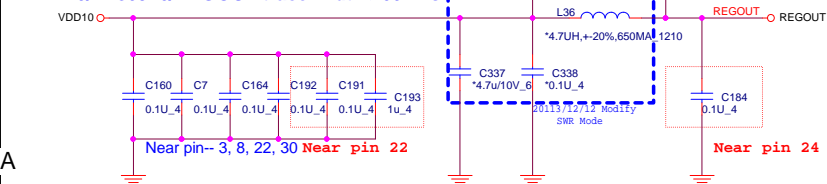
RJ45(LAN)

RTL8161 Add C335, C336
RTL8151 Del C335, C336

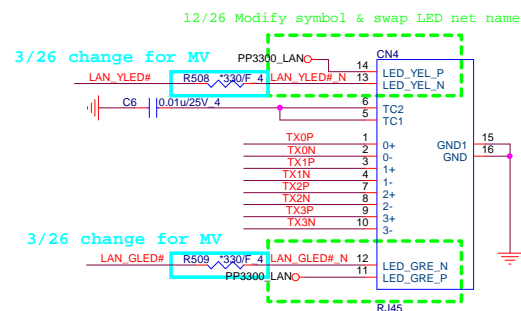
EVDD10/AVDD33_REG trace width >60mils



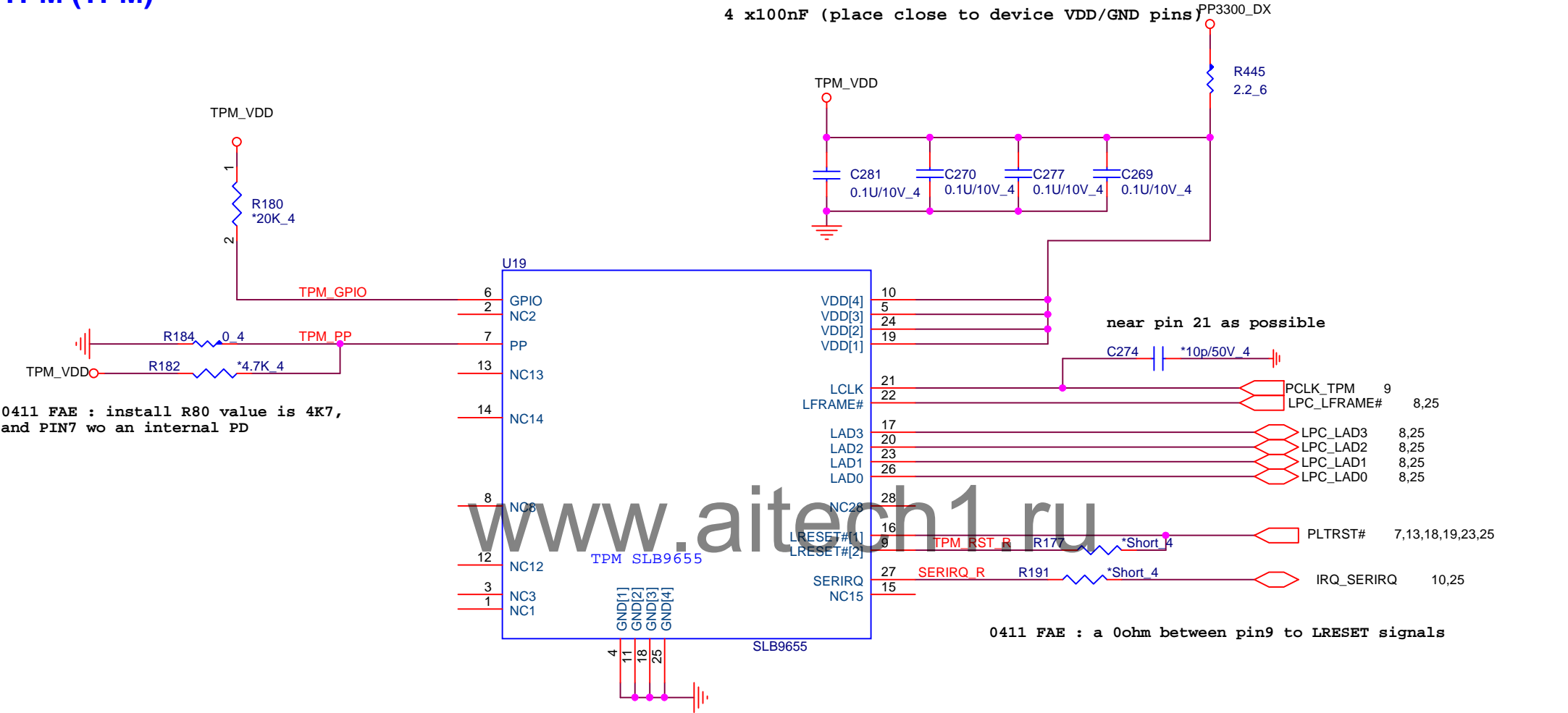
EVDD10/N780946/REGOUT trace width >60mils




RTL8161 Add L36, C337, C338
RTL8151 Add R43, C184 Del L36, C337, C338



TPM (TPM)



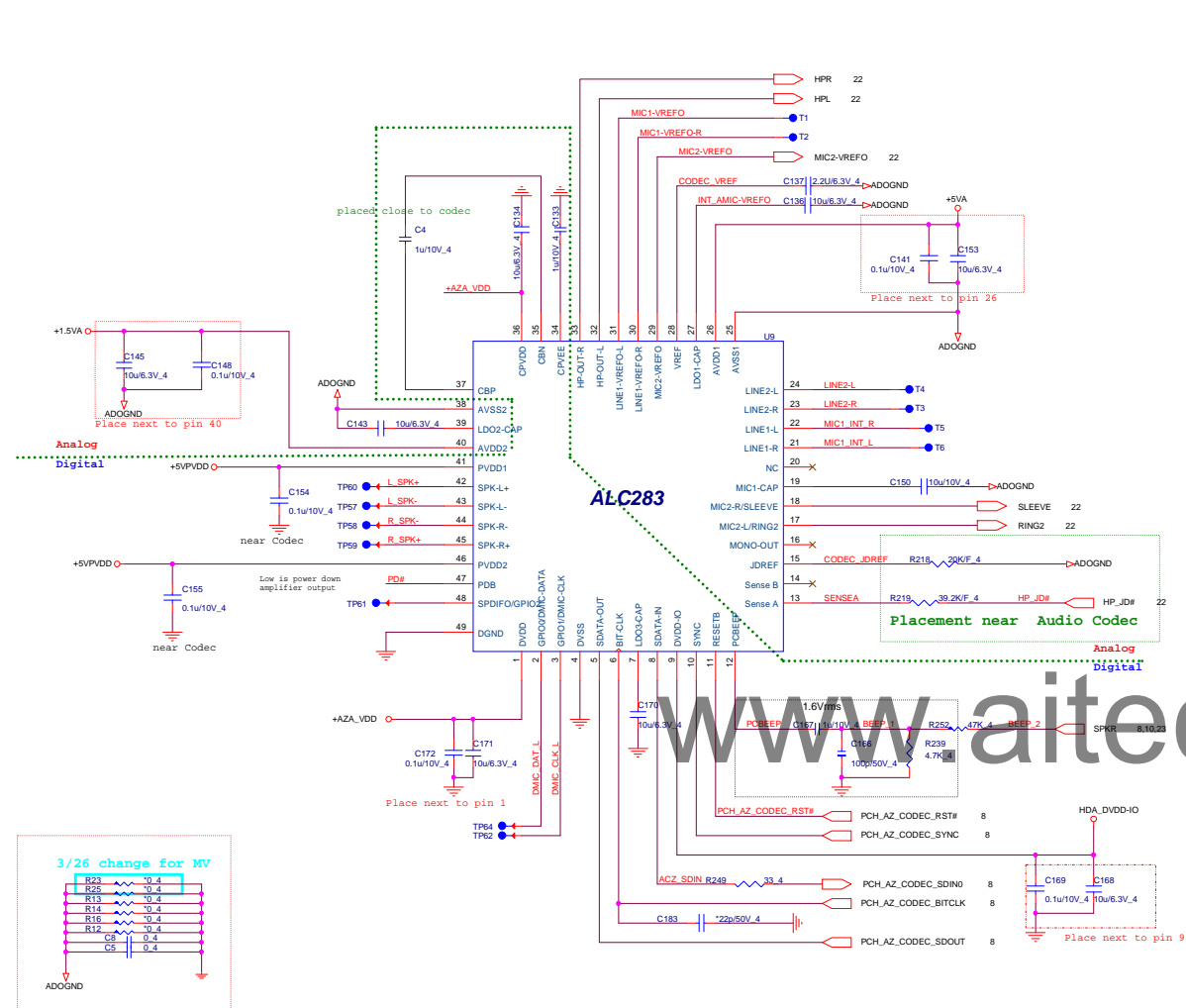


Quanta Computer Inc.

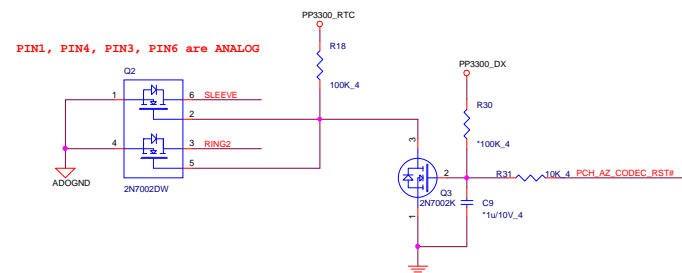
PROJECT : 0W9

Size	Document Number	Rev 3A
TPM SLB9655 / LED		
Date:	Monday, March 31, 2014	Sheet 20 of 33

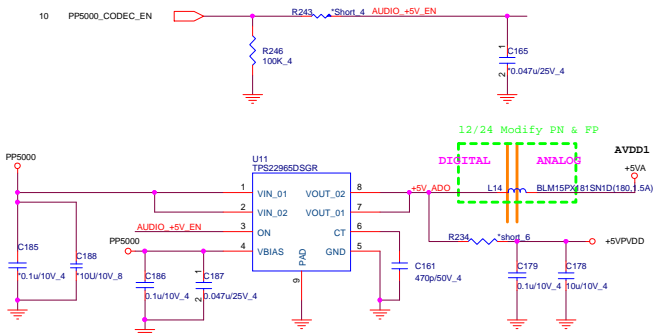
Codec(ADO)



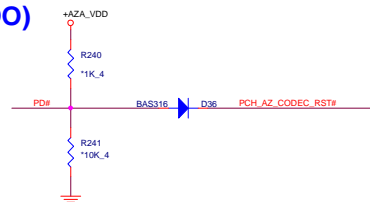
Grounding circuit(ADO)



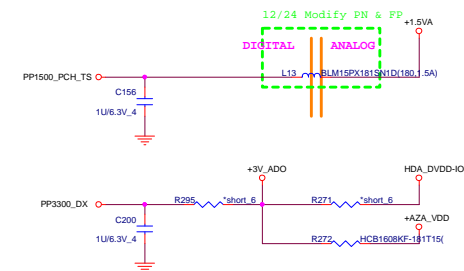
Codec PWR 5V(ADO)



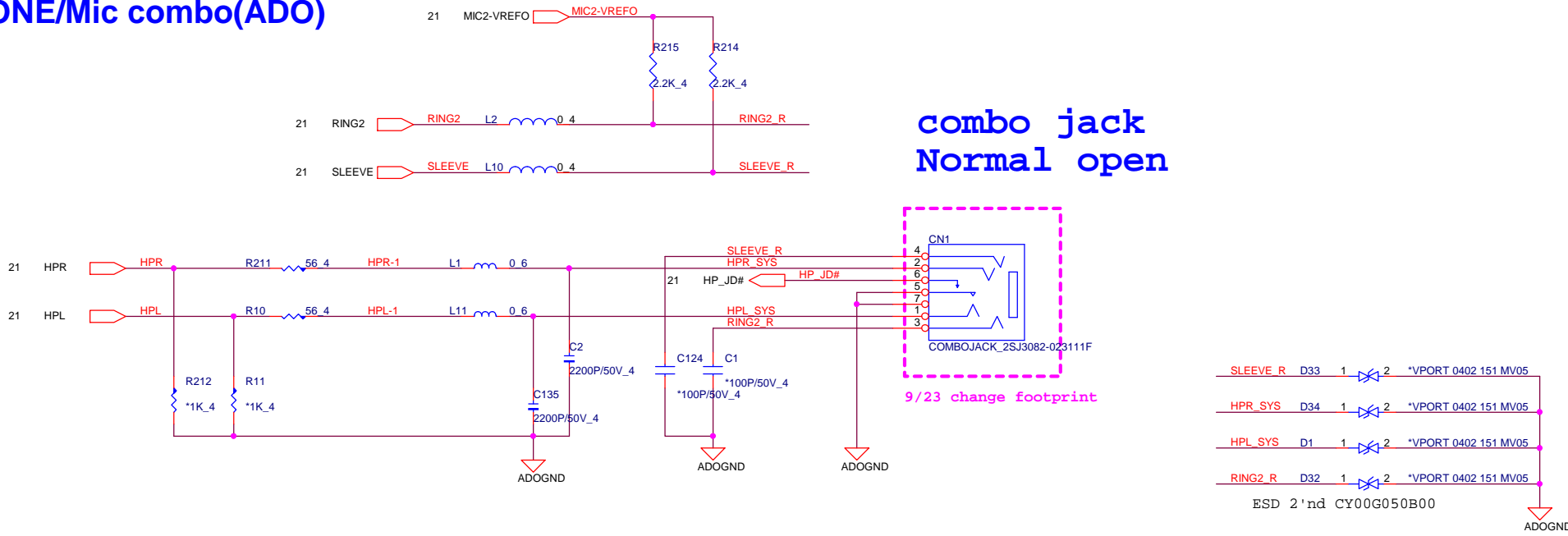
Mute(ADO)




Codec PWR 3V/1.5V(ADO)



HEADPHONE/Mic combo(ADO)

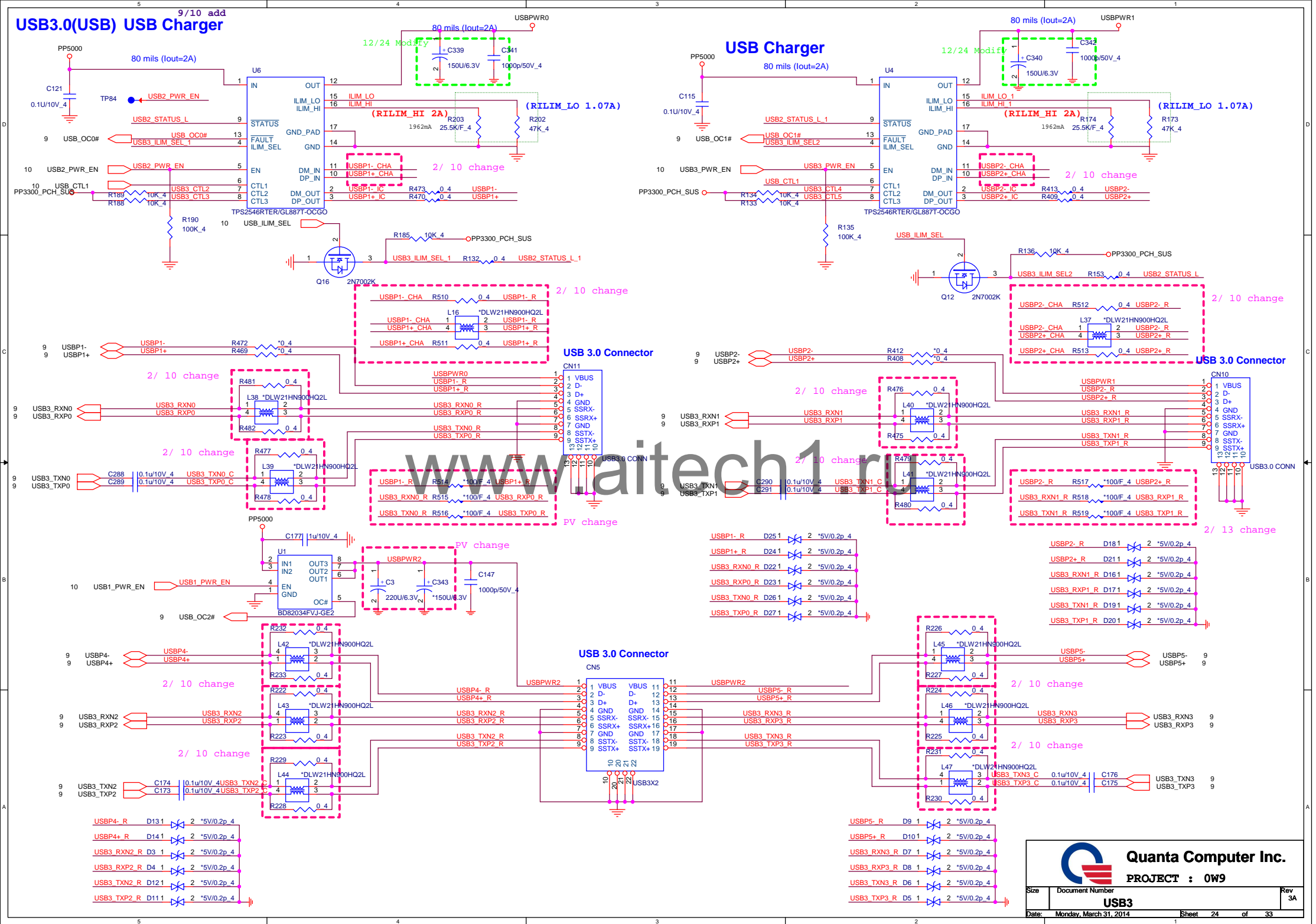


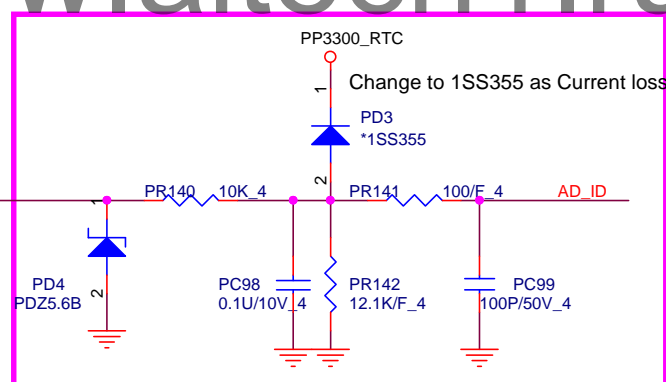
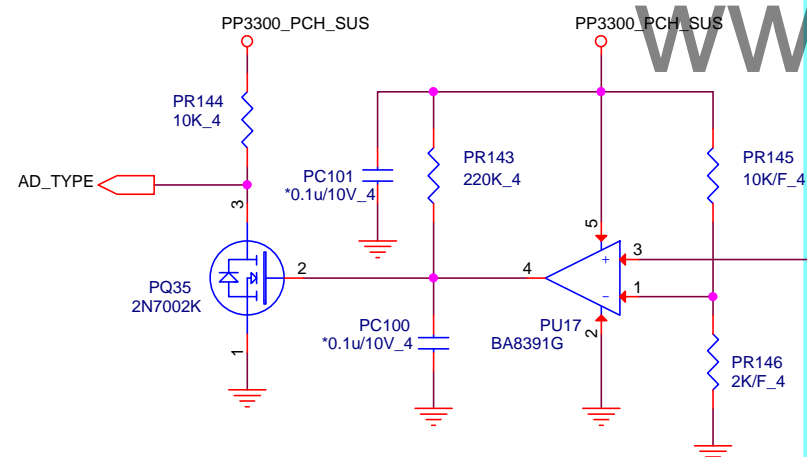
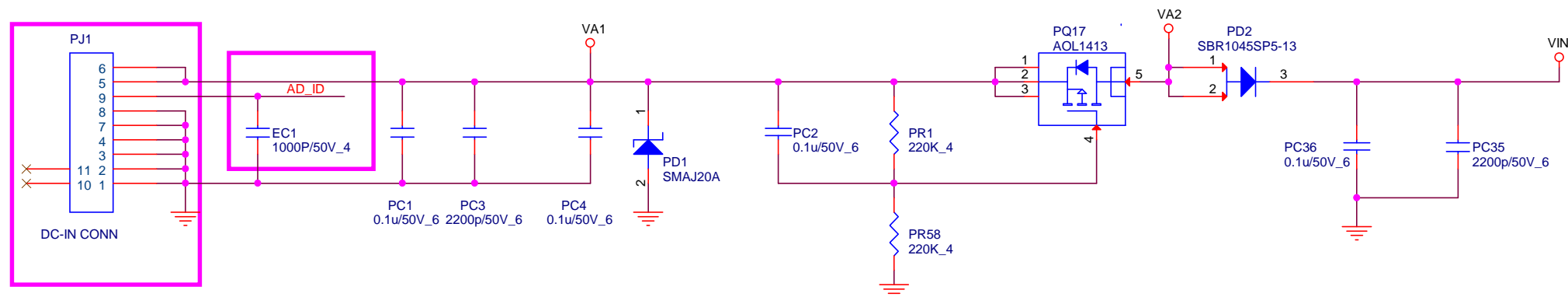
www.aitech1.ru

		Quanta Computer Inc.	
		PROJECT : 0W9	
Size	Document Number	Rev 3A	
Audio Headset SW			
Date:	Monday, March 31, 2014	Sheet	22 of 33

9/10 add

USB3.0(USB) USB Charger





Quanta Computer Inc.

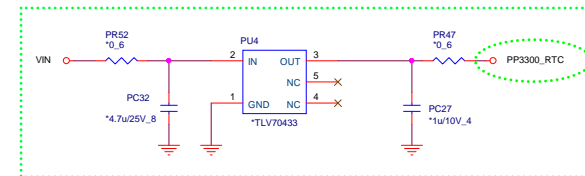
PROJECT : 0W9

Size	Document Number	Rev
	DC-IN	3A
Date:	Monday, March 31, 2014	Sheet 26 of 33

PP3300_LAN_EN_D → PP3300_LAN_EN_D 31
 PP3300_WLAN_EN_D → PP3300_WLAN_EN_D 31
 PP3300_VPB_EN_D → PP3300_VPB_EN_D 31

MAIND → MAIND 28,31
 SSD → SSD

2013/8/20 PP3300_RTC



3.3 Volt +/- 5%
 TDC : 4A
 PEAK : 5.4A
 Width : 160mil

TDC : 0.15A
 PEAK : 0.2A
 Width : 20mil

www.aitech1.ru

For PP5000_DSW (S5)

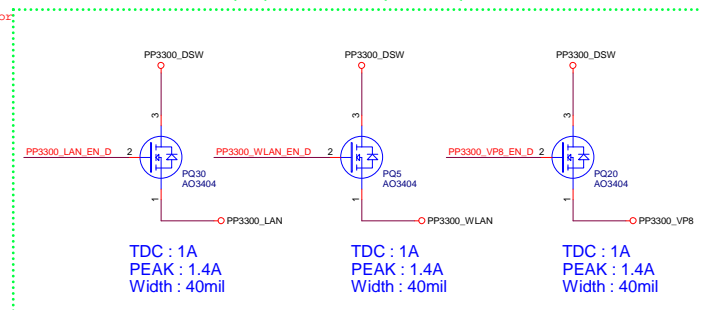
For PP5000_DSW (ALW)

PP5000_DSW
 MAIND → MAIND 2
 +5V

TDC : 0.4A
 PEAK : 0.54A
 Width : 20mil

TDC : 0.56A
 PEAK : 0.74A
 Width : 40mil

2013/8/20 LAN/WLAN/VP8 decoder

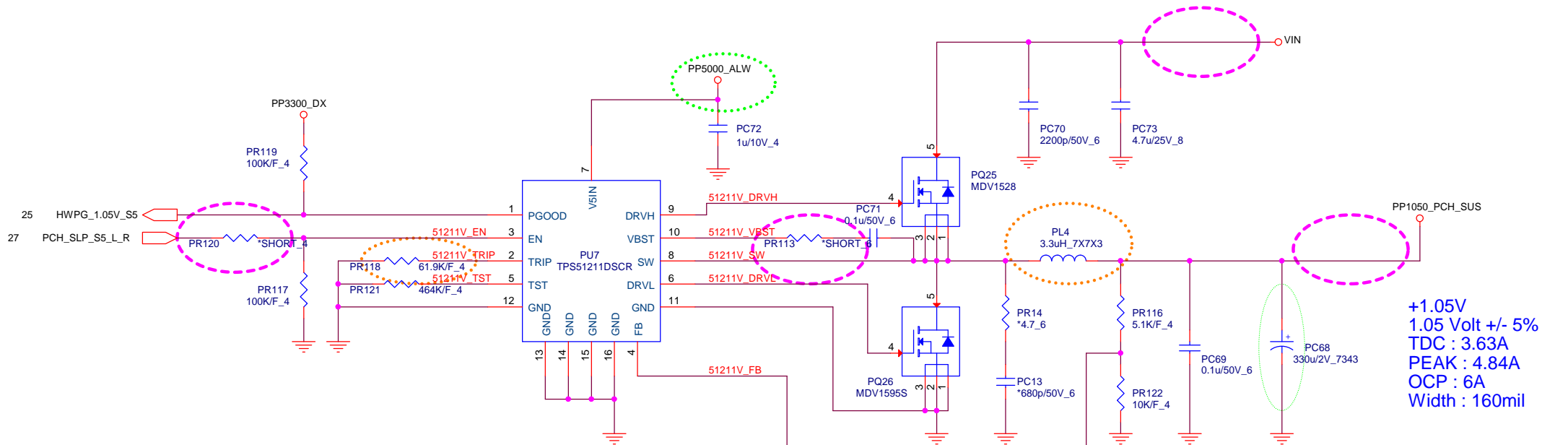


TDC : 1A
 PEAK : 1.4A
 Width : 40mil

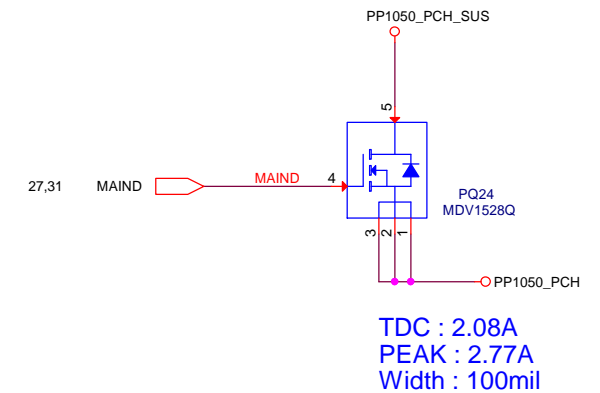
TDC : 1A
 PEAK : 1.4A
 Width : 40mil

TDC : 1A
 PEAK : 1.4A
 Width : 40mil

7 PCH_SLP_SUS_L → R491 *SHORT_4 PCH_SLP_SS_L_R → PCH_SLP_SS_L_R 28
 7.13 PCH_SLP_SS_L → PCH_SLP_SS_L R490 *0.4



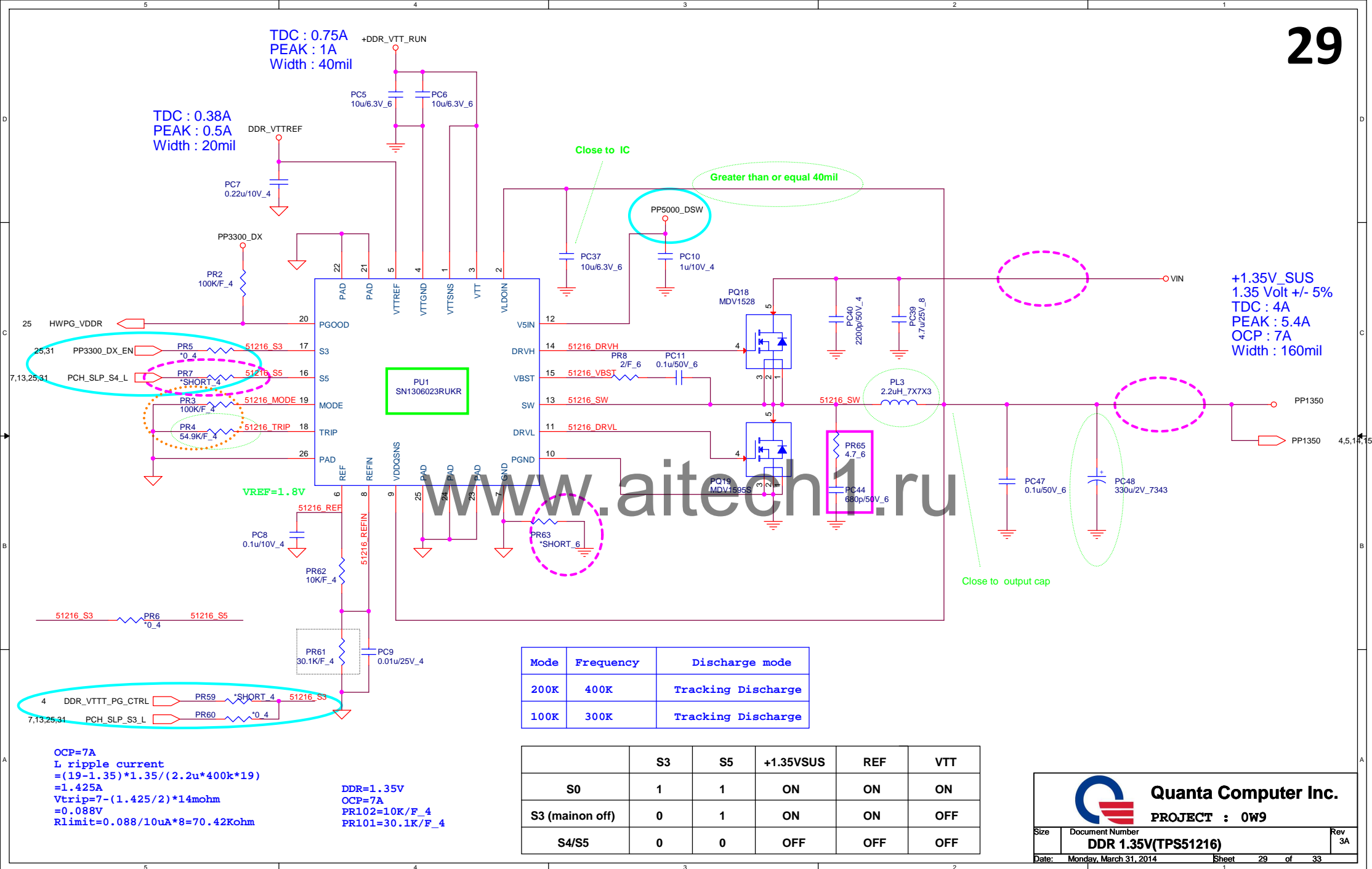
OCP=6A
 L ripple current
 $= (19-1.05) \cdot 1.05 / (2.2 \mu \cdot 290k \cdot 19)$
 $= 1.555A$
 $V_{trip} = 6 - (1.555/2) \cdot 14mohm$
 $= 0.0731V$
 $R_{limit} = 0.0731 / 10 \mu A \cdot 8 = 58.49Kohm$

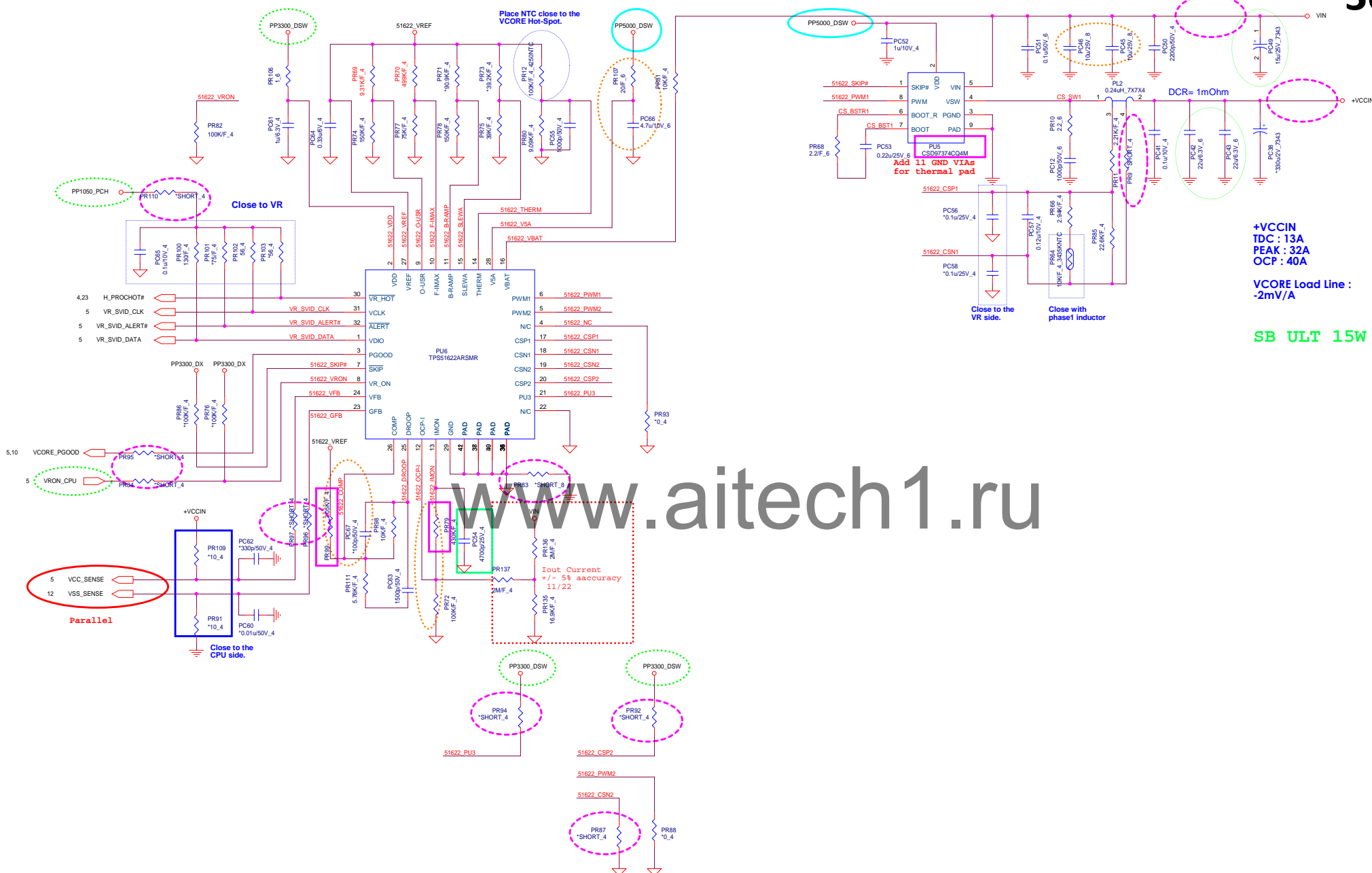


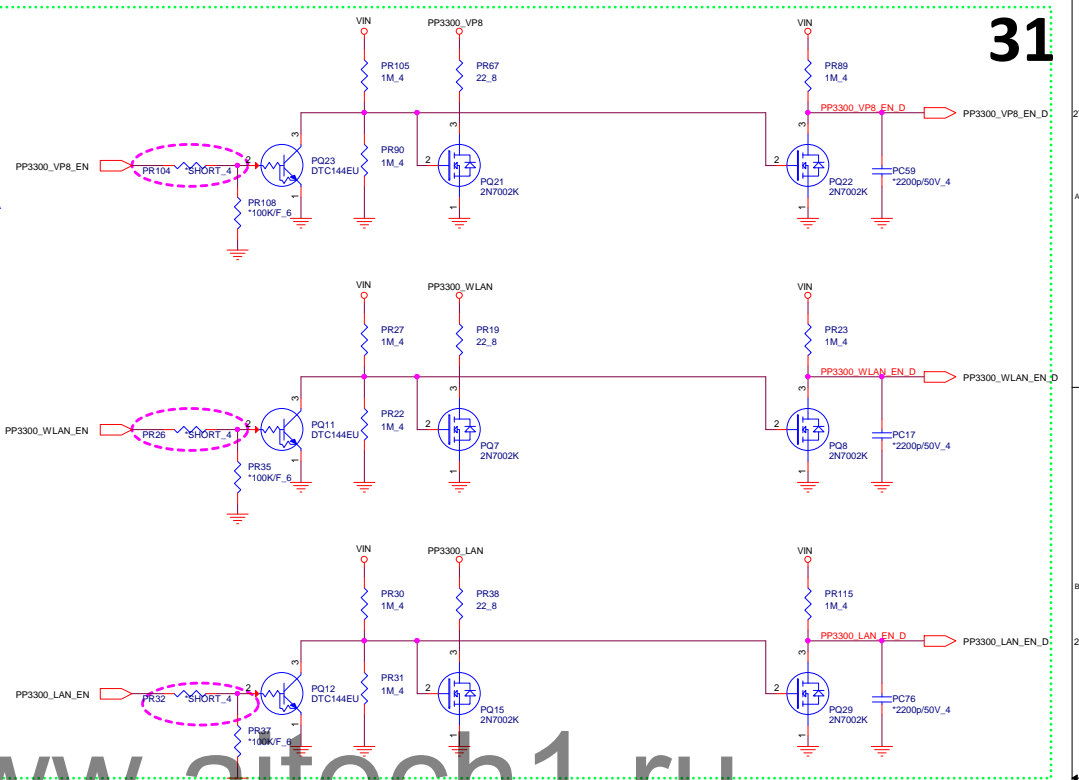
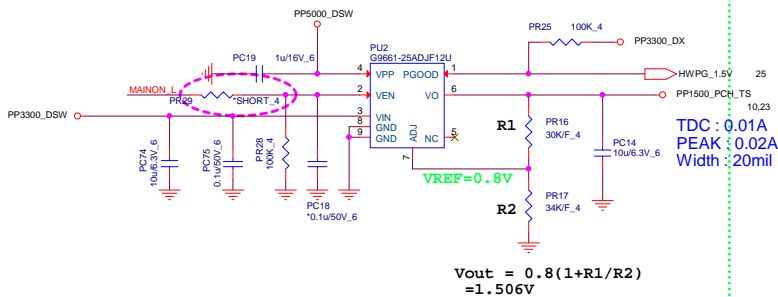
Quanta Computer Inc.
PROJECT : 0W9

Size	Document Number	Rev
	+1.05V(TPS51211)	3A

Date: Monday, March 31, 2014 Sheet 28 of 33







www.aitech1.ru

